Networks on Chips: 15 Years Later

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The authors of a Computer *article from 2002 reflect on their proposal to use networks on chips to address scalable communications on silicon VLSI chips.*

FROM THE EDITOR

As part of our 50th anniversary celebration, this special feature revisits influential *Computer* articles from the past. This month, the original authors of "Networks on Chips: A New SoC Paradigm" from the January 2002 issue discuss their article and how virtually all large-scale chips are now designed with this paradigm. *–Ron Vetter, Editor in Chief Emeritus*

When it became clear that communication means are crucial for computing performance and energy consumption, we, along with other researchers, began performing system-level analysis of power-efficient multiprocessing in silicon. As a result of this analysis, we proposed the concept of networks on chips (NoCs) in this magazine as a general paradigm to realize modular and scalable communication on silicon VLSI chips ("Networks on Chips: A New SoC Paradigm," *Computer*, vol. 35, no. 1, 2002, pp. 70–78).

Although our work benefitted from interactions with colleagues at Stanford University and inspiration from activities at the University of California, Berkeley, and Pierre and Marie Curie University, we chose a specific constructive approach to NoC design. We created methods, tools, and flows to realize NoCs as structured interconnects, using synthesis tools such as Xpipes and XpipesLite (prototypes from the University of Bologna and Stanford) and simulation tools such as MPARM.

Whereas VLSI circuits of the 1990s were put together by placing and routing cells from a cell library, current VLSI systems are designed by networking high-level models of processors and memory. The required raise in abstraction level is dictated by the systems' increased complexity and by the need to optimize the systems' performance and energy to be competitive and to avoid dark silicon issues.

This approach has been tremendously successful. Today, virtually all large-scale chips are designed with NoCs. Starting with Intel's groundbreaking Polaris 80-core Teraflops processor prototype in 2006, most silicon vendors design, manufacture, and sell products based on NoCs. Notable examples include STMicroelectronics' STHORM processor (2012), featuring an asynchronous NoC and delivering 40 giga operations per second per watt in 28-mm bulk technology; Altera's Arria 10 system-on-chip (SoC)

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field-programmable gate array (FPGA) family, using Arteris's FlexNoC interconnect (2014); and IBM's TrueNorth neuromorphic 5.4-billion transistor chip, where 4,096 neurosynaptic cores are networked together (2014). Arteris is a major commercial NoC tool provider and FlexNoC is their suite for analyzing, synthesizing, and optimizing NoCs. Qualcomm bought FlexNoC in 2013, but Arteris continues to operate and support its customers, which include major semiconductor houses. Thus, NoCs are part of a large number of products that we use every day. These examples show that the NoC paradigm is scalable and broad, and that it can be adapted to support various computational paradigms, ranging from multiprocessing to reconfigurable computing and the emerging area of neuromorphic computing.

New groundbreaking application areas, like autonomous self-driving cars, require adaptive high-performance multiprocessing where NoCs constitute the ideal communication fabric. Indeed, on-chip communication must satisfy various timing constraints, such as latency-critical execution paths (for emergency braking control) as well as high-bandwidth links (for feeding video data from cameras to processors and memory). NoCs embody the best design solution because of their flexibility to accommodate constraints and because they are easy to design and verify. Mobileye's (now Intel's) Driver Assistance System was designed with FlexNoC, and NVIDIA recently announced the Parker processor and the Drive PX2 platform for autonomous vehicles, using a coherent on-chip fabric to achieve distributed cache-coherent NoCs.

Over the past several years, NoCs have also been used to support emergent technologies. A joint collaboration lead by France's CEA-Leti demonstrated the use of a scalable 3D NoC for multiple silicon-layer integrated circuits (ICs) connected by through-silicon vias. Such an NoC supports a 326 mega flits per second data rate with an energy cost of 0.66 picojoules per bit. Researchers at leading academic and industrial labs have realized the key building blocks for optical NoCs, combining photonic transducers with silicon modules to achieve higher bandwidth at single-digit picojoules per bit energy-efficiency levels.

The broad application of NoCs in IC design has been enabled by NoC synthesis tools that evolved from university prototypes to full commercial synthesis flows. NoC synthesis tools enable designers to describe communication requirements and constraints at a high level of abstraction and produce register-transfer-level descriptions of the NoC building blocks that are amenable to synthesis and validation through standard electronic design automation tools. Introducing NoCs has also spurred an incredibly large number of research activities in academia and industry worldwide because of the multitude of networking solutions and technological constraints they can address.

ARCHIVED ARTICLES

The authors' original article postulating that the layered design of reconfigurable micronetworks can achieve efficient communications in system-on-chip designs remains very popular, as indicated by the number of downloads it receives from the IEEE Computer Society Digital Library. All of the original articles mentioned in this special column are free to view at www.computer.org/computer-magazine/from-the-archives-computers-legacy.

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