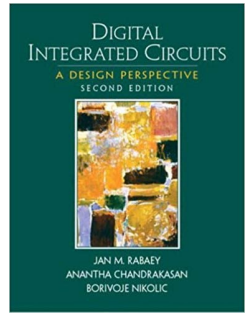
Microeletrônica

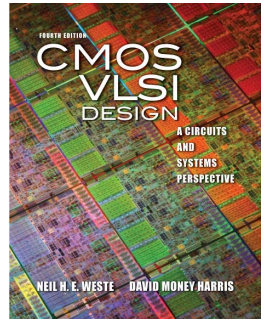
Aula #8 → Circuitos sequenciais dinâmicos

- Professor: Fernando Gehm Moraes
- Livro texto:

  Digital Integrated Circuits a Design Perspective - Rabaey

  C MOS VLSI Design - Weste

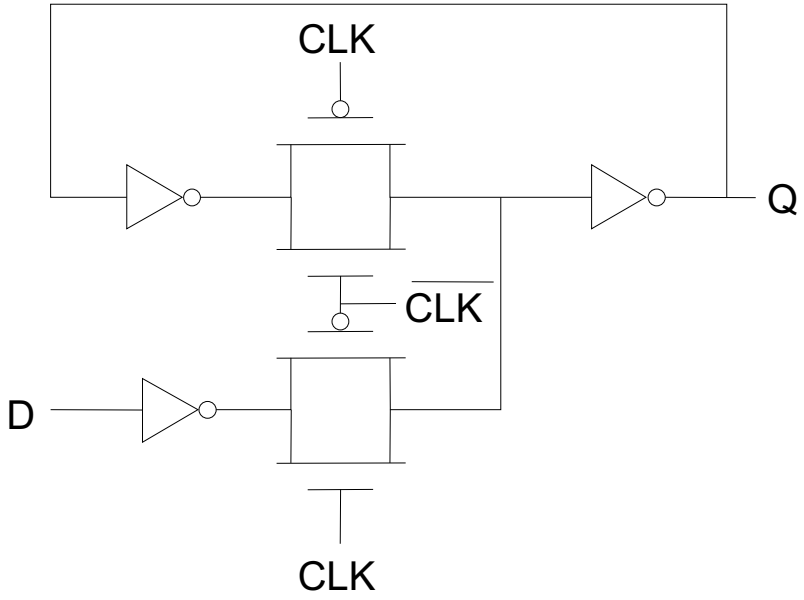




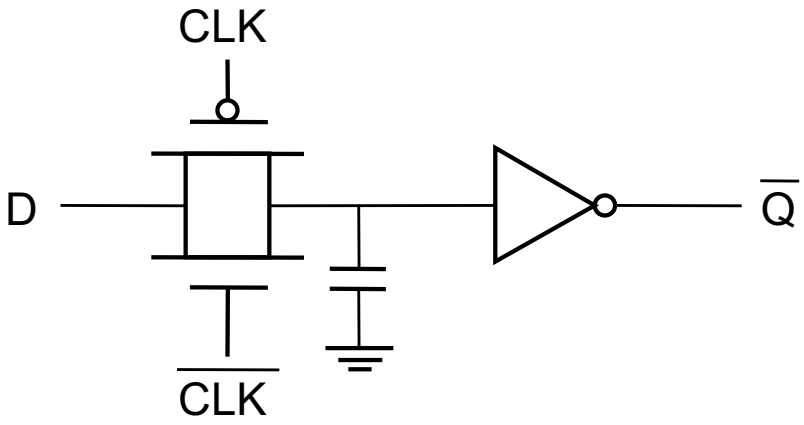
Revisão das lâminas: 09/maio/2025

Storage Mechanisms

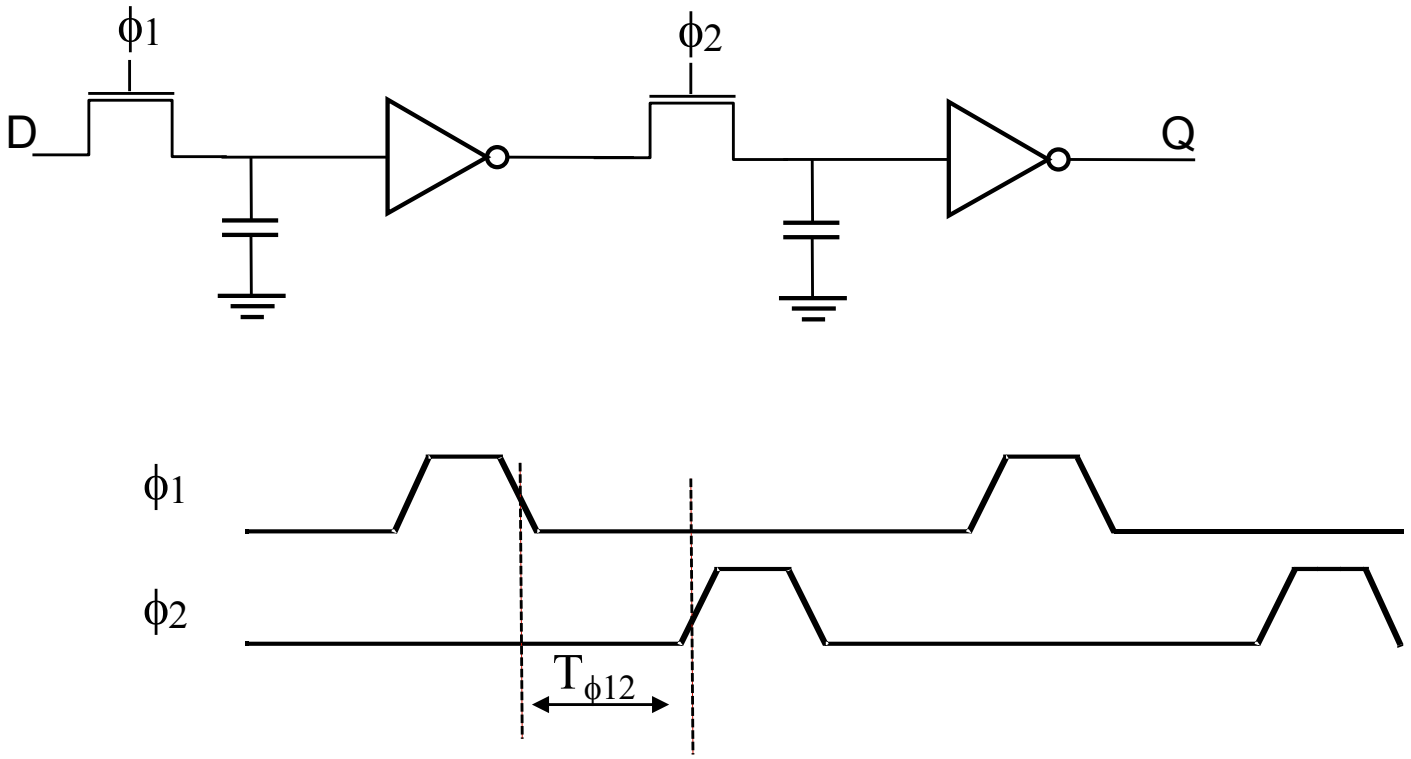
Static (mux-based latch)



Dynamic (charge-based)

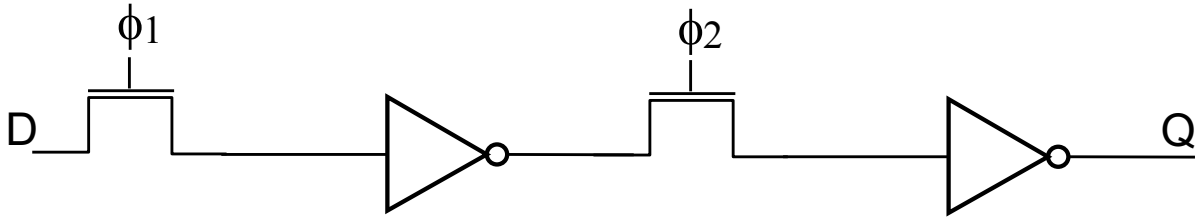


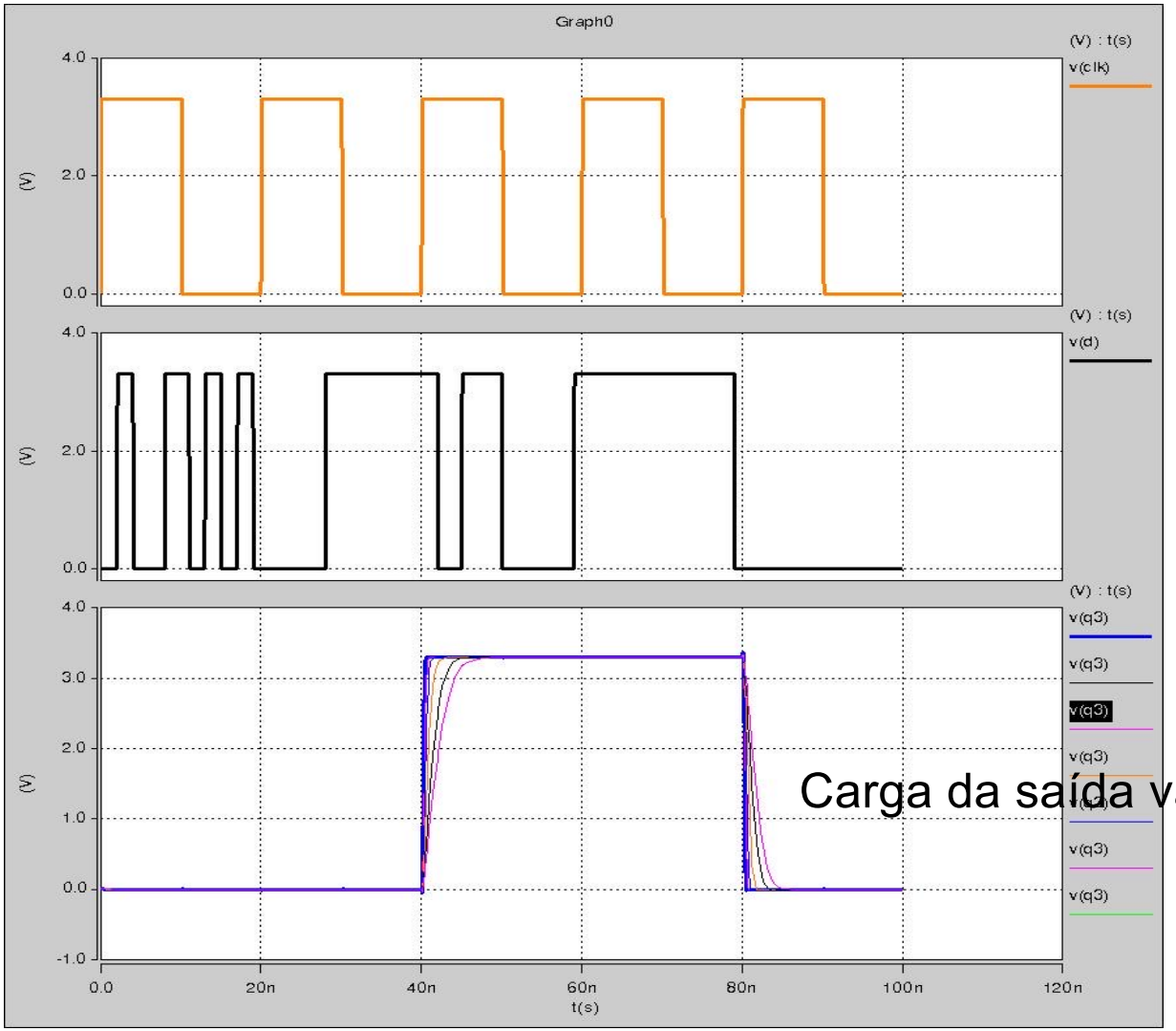
Flip Flop MS Dinâmico de 2 Fases



- Reduzida complexidade dos circuitos dinâmicos
- A implementação necessita somente 6 transistores
- Necessita relógios sem sobreposição
- $T_{\phi 12}$ pode ocasionar perda de desempenho

Simulação






```
.subckt din d q ck vcc
X1 d   nck   ck A vcc tg
X2 A   B           vcc inv
X3 B   ck   nck C vcc tg
X4 C   q           vcc inv
X5 ck nck    vcc inv
.ends din
```

Carga da saída variando de 5 a 50fF

FF Mestre-Escravo: C²MOS

MS dinâmico insensível à sobreposição das fases de clock

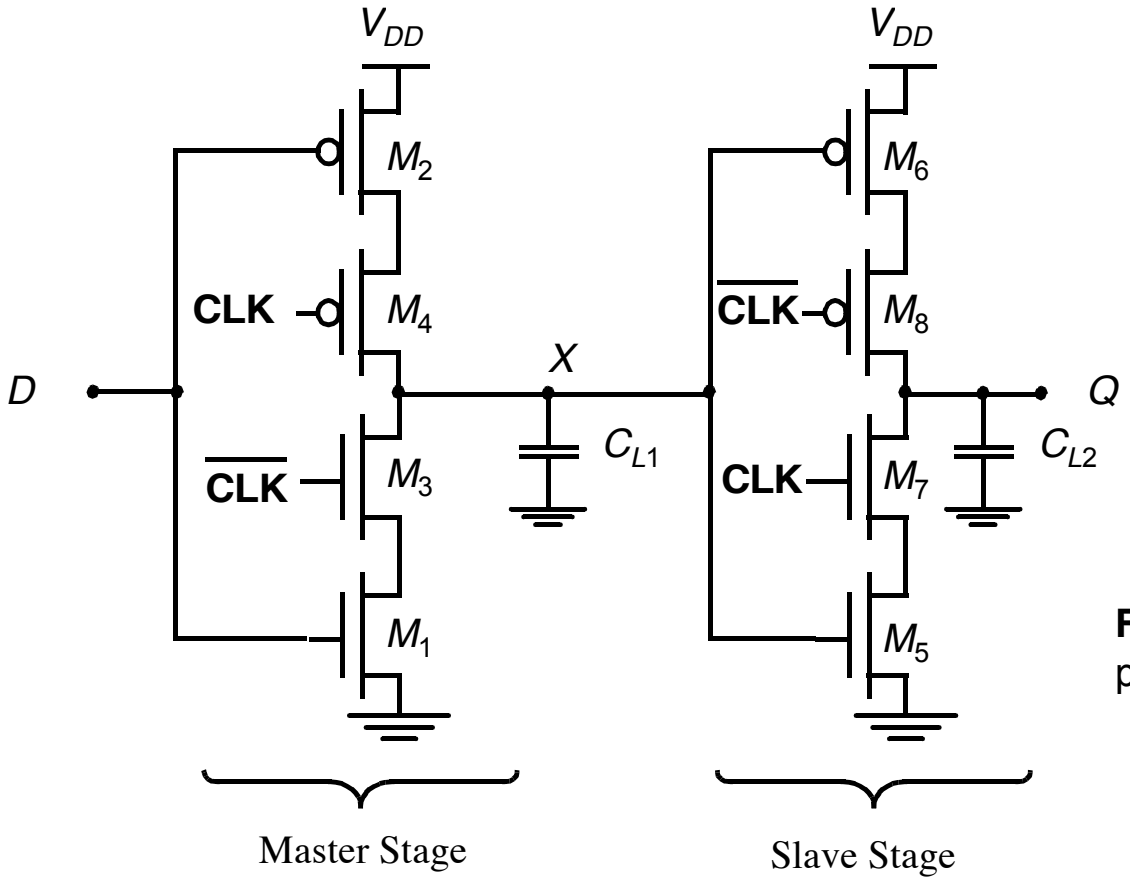
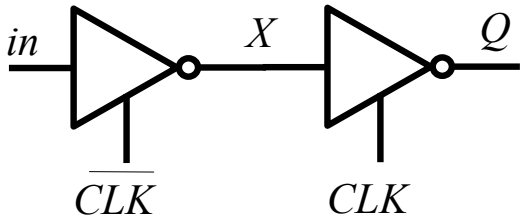


Figure 7.26 C²MOS master-slave positive edge-triggered register.



Insensitive to Clock-Overlap

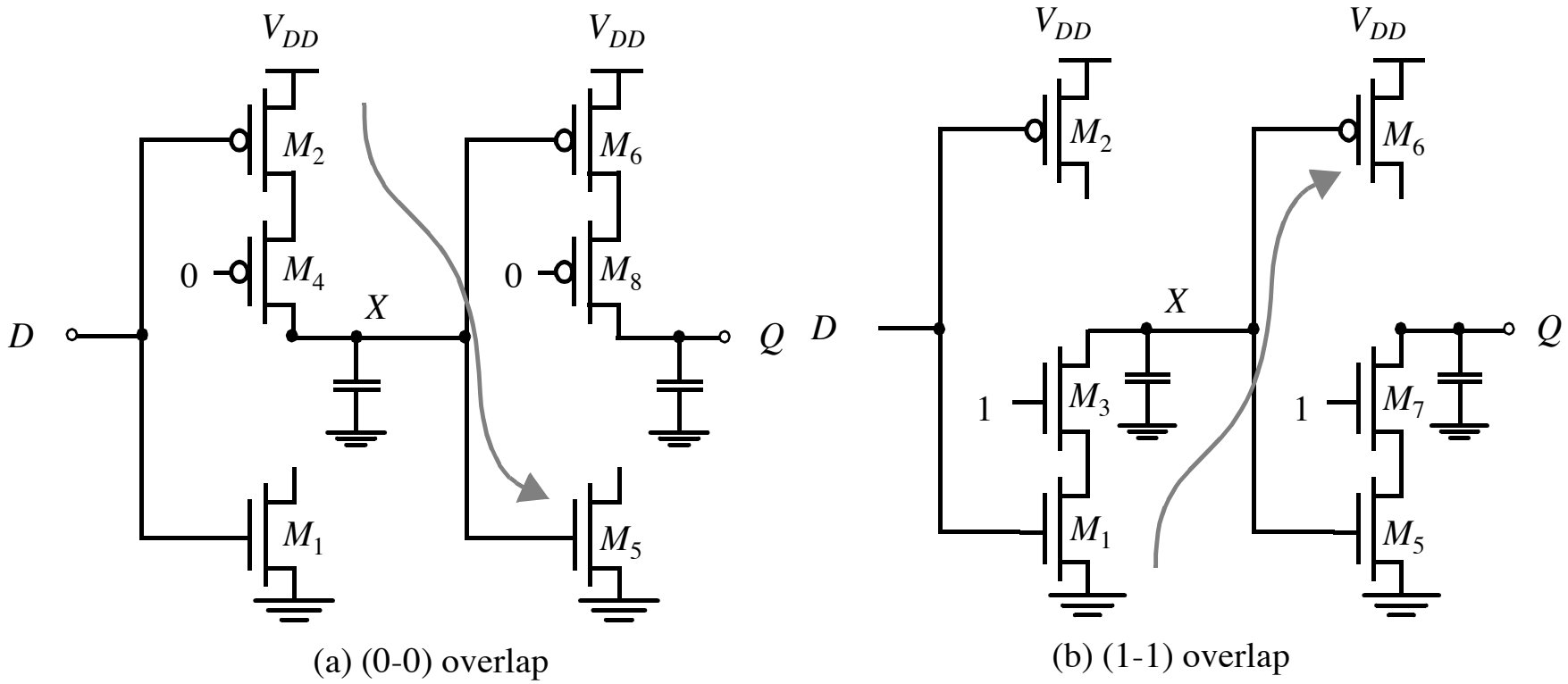
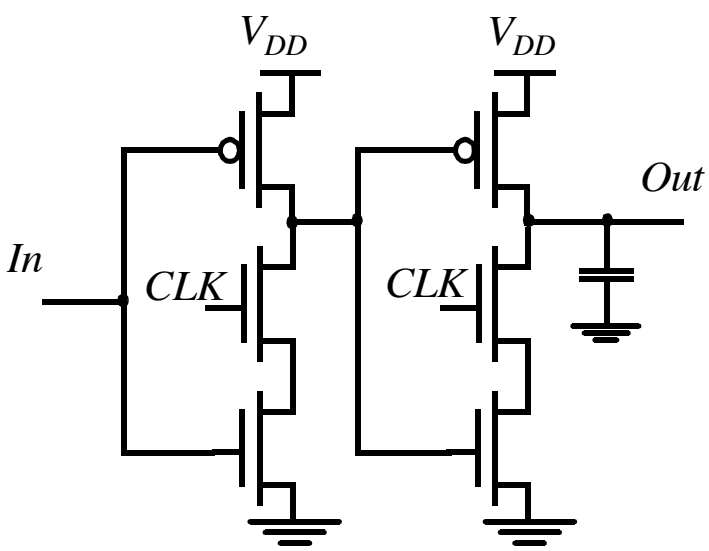


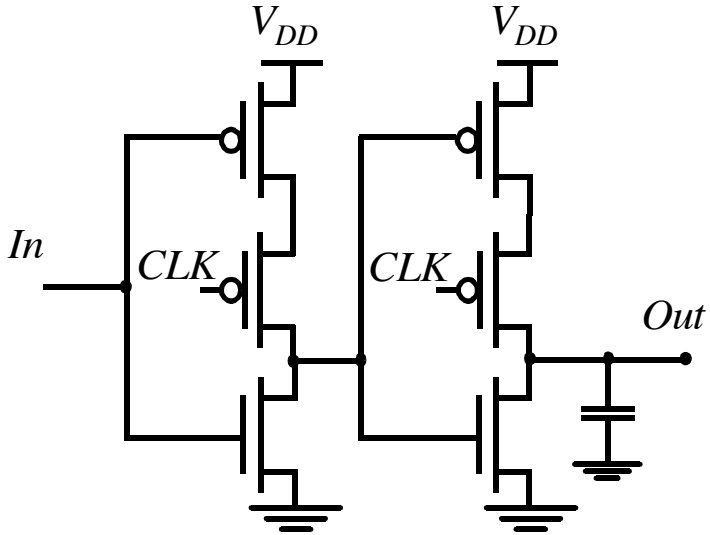
Figure 7.27 C^{2}MOS *D*-FF during overlap periods. No feasible signal path can exist between *In* and *D,* as illustrated by the arrows.

Latch TSPC

TSPC → True Single-Phase Clocked



Positive Latch



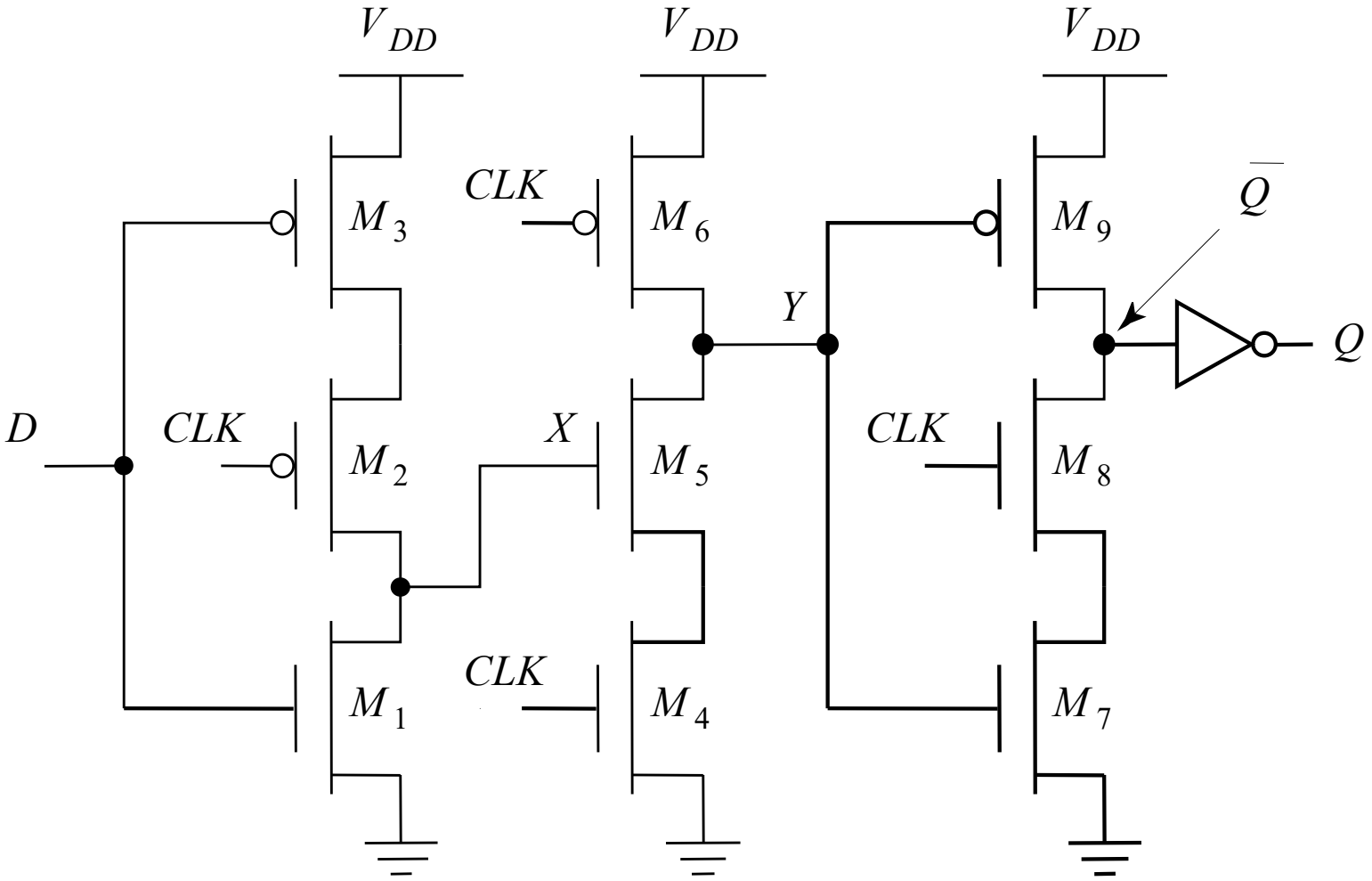
Negative Latch

Figure 7.30 True Single Phase Latches.

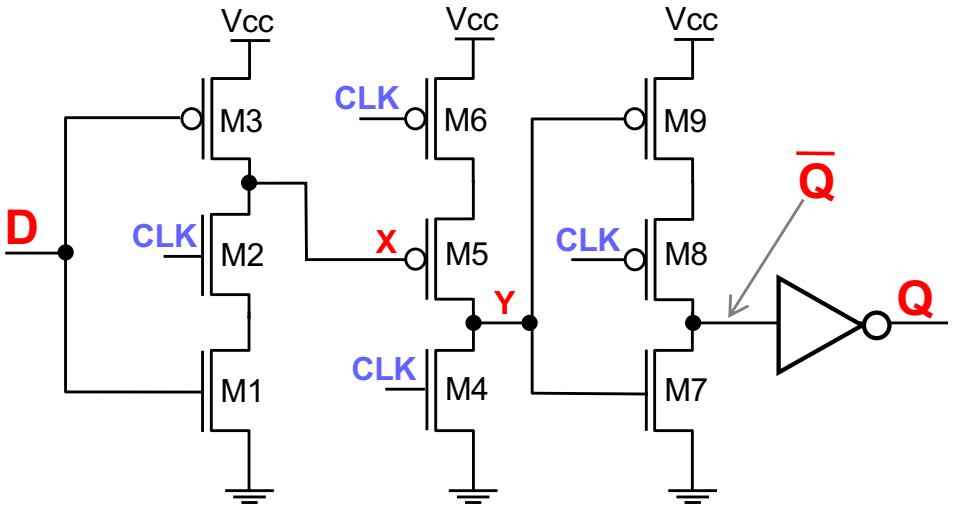
Positive latch (transparent when CLK= 1)

Negative latch (transparent when CLK= 0)

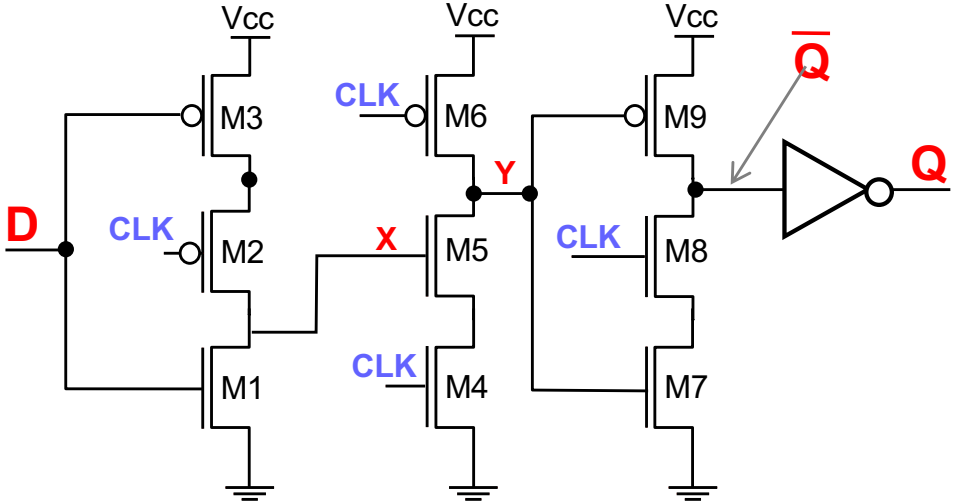
Mestre-escravo TSPC - subida



Mestre-escravo TSPC



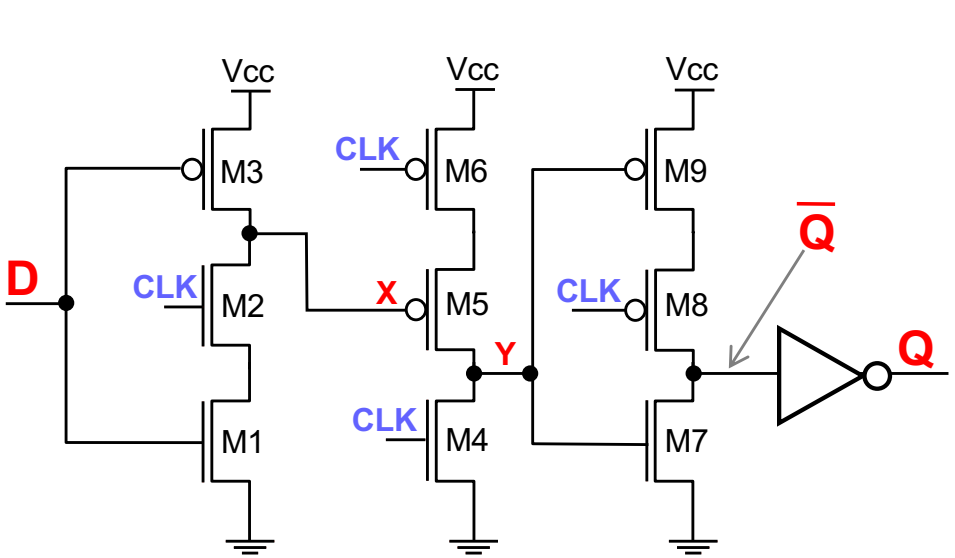
descida

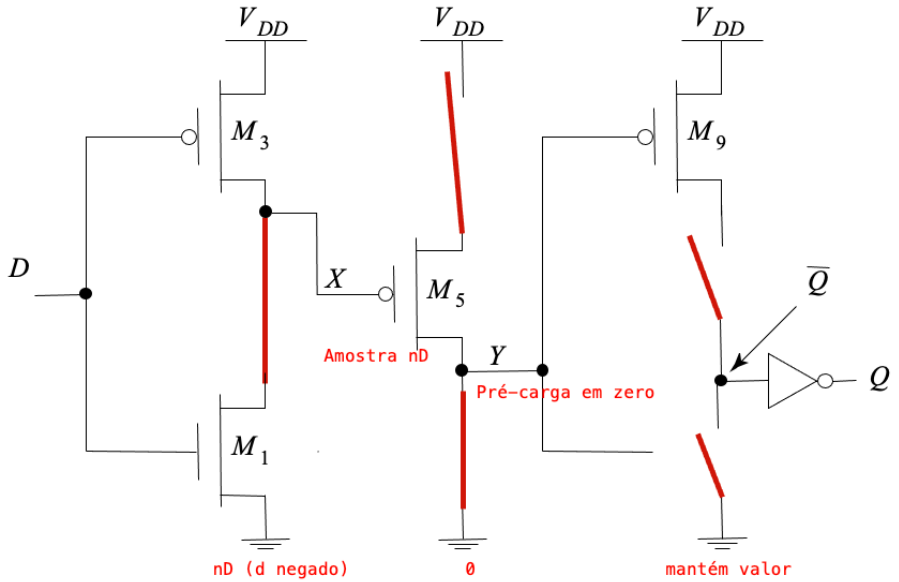


subida

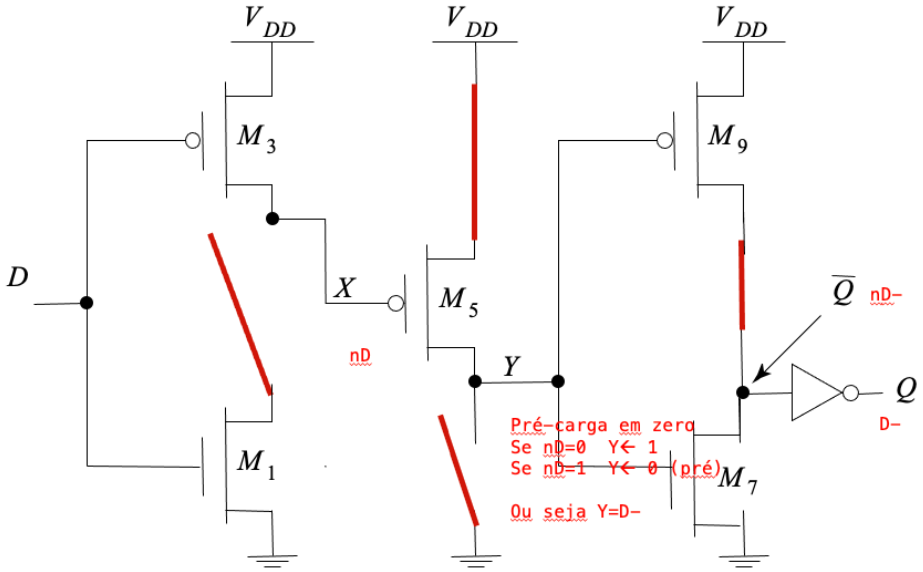
Possui a vantagem de necessitar um único relógio

CK=1: amostra em M5, pré-carga 0 em Y, mantém Q





CK= ⇩: Y recebe D antes da borda, e transfere para saída



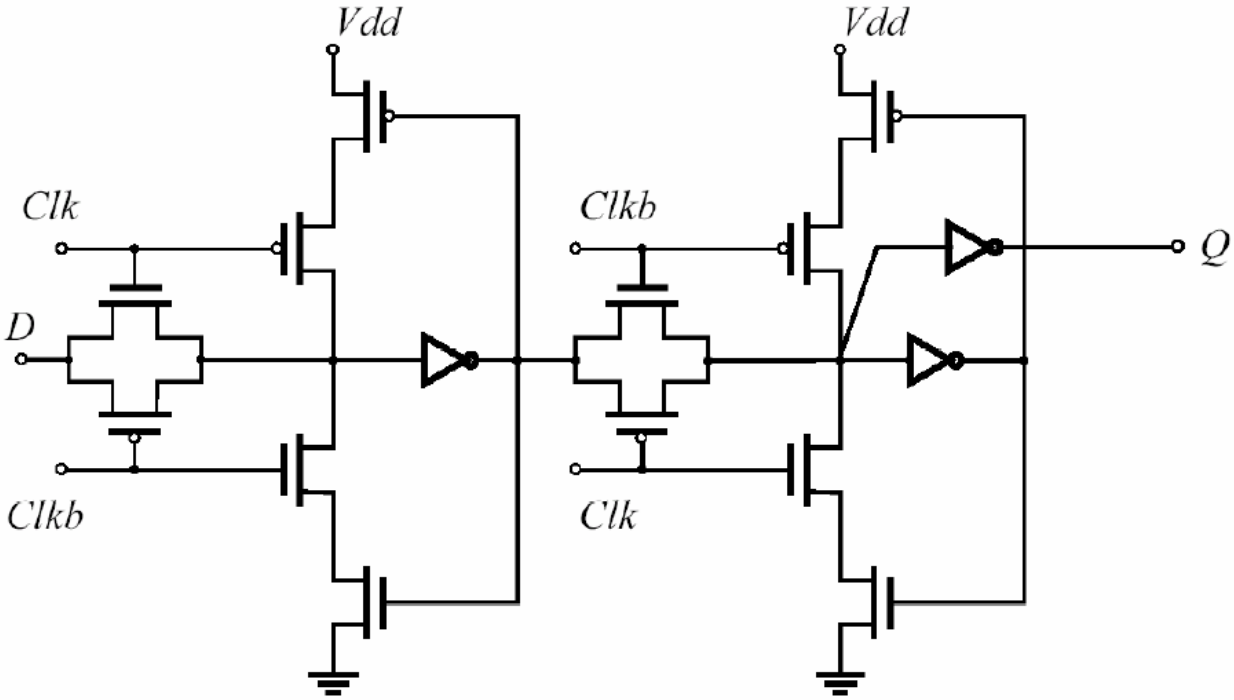
Exercício – analise o seguinte FF

- Fonte: **http://www.ece.ncsu.edu/asic/ece733/2008/docs/FlipFlops1up.pdf**

Transmission Gate Master-Slave

PowerPC 603

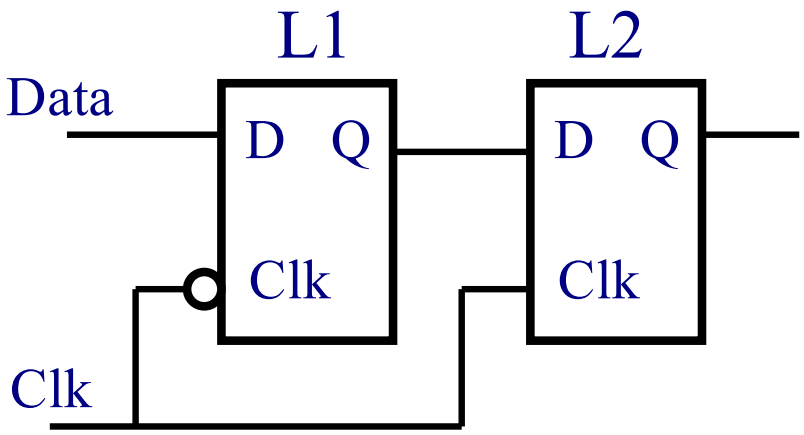
- Clock Load
  - High
- Power
  - Low
  - low power feedback
- Positive setup



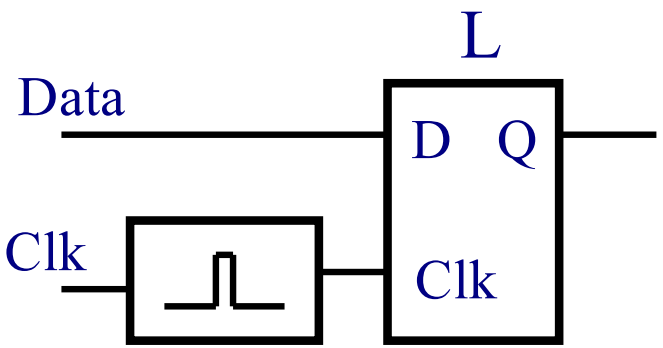
Pulse-Triggered Latches
An Alternative Approach

Ways to design an edge-triggered sequential cell:

Master-Slave Latches

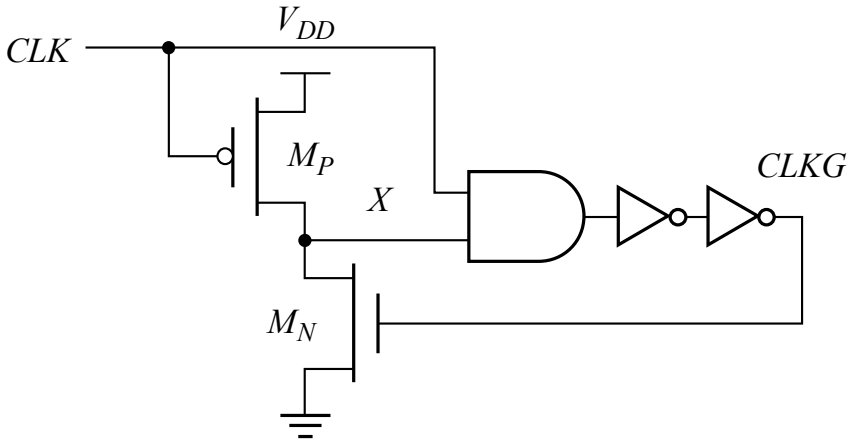


Pulse-Triggered Latch

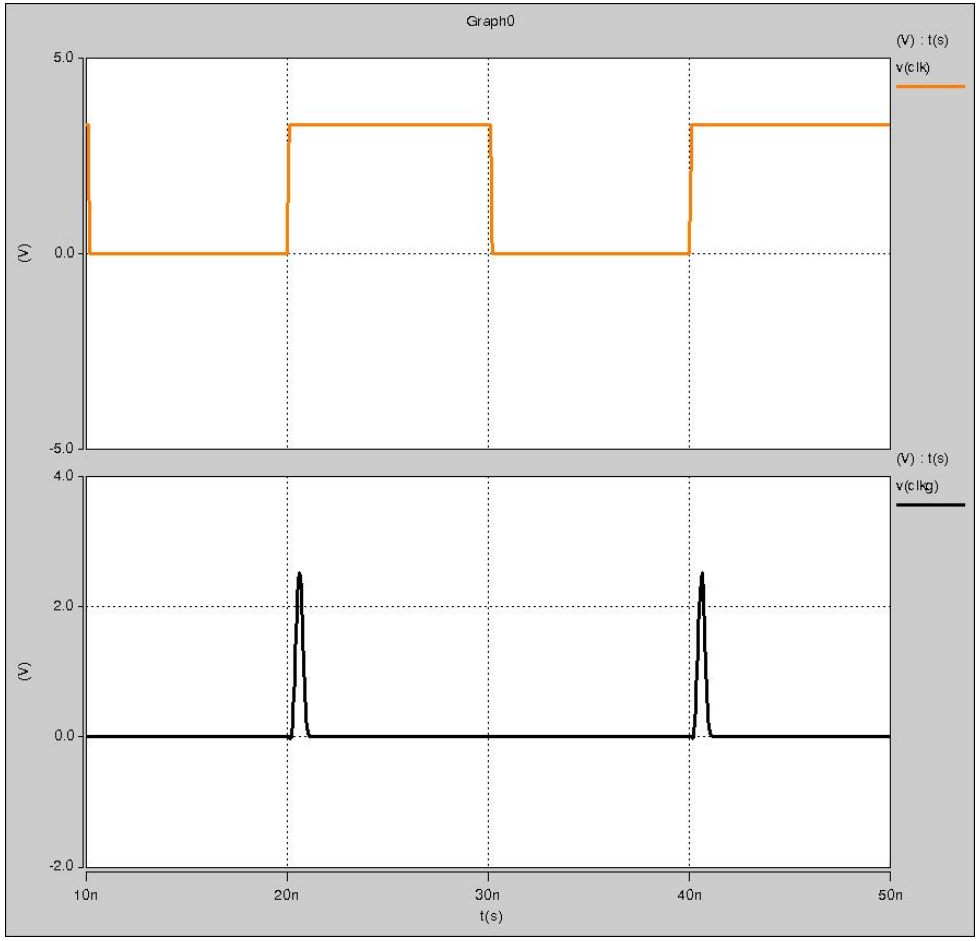


Circuito Gerador de Pulso

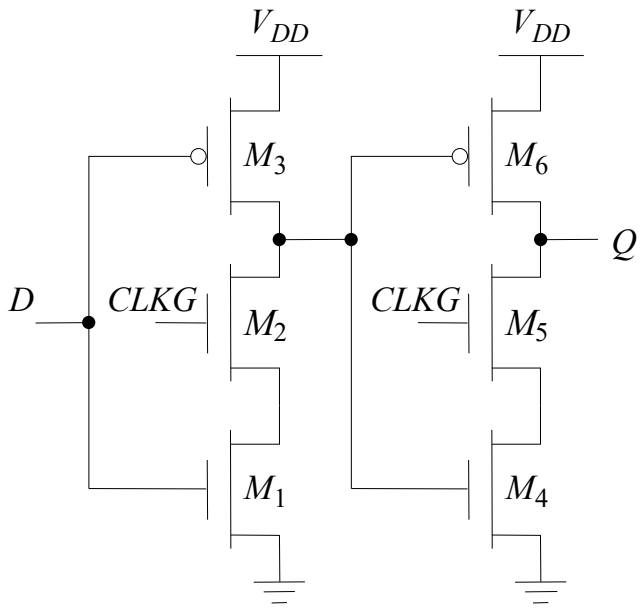
- A idéia é não usar MS, e sim latches, usando como gatilho pulsos muito rápidos



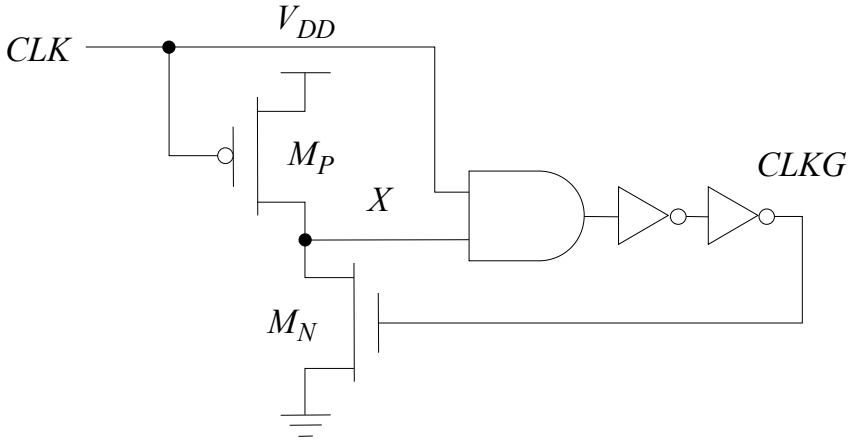

```
.subckt pulso clk clkg vcc
X1 clk  X n1 vcc nand2
X2 n1 clkg     vcc inv
MP2 X  clk vcc vcc pmos l=0.35U W=3.0U
MN2 X  clkg  0 0   nmos l=0.35U W=1.5U
.ends pulso
```



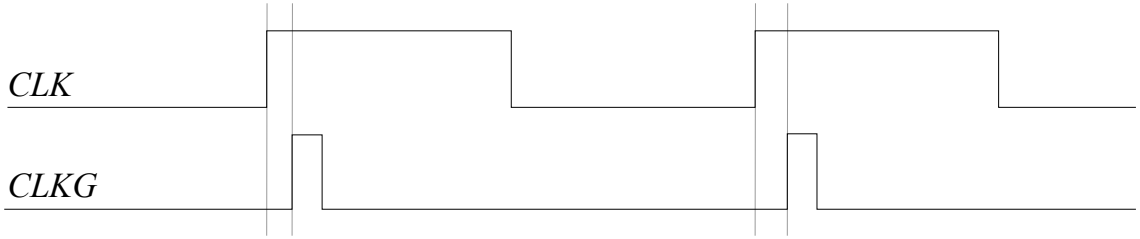
Pulsed Latches



(a) register



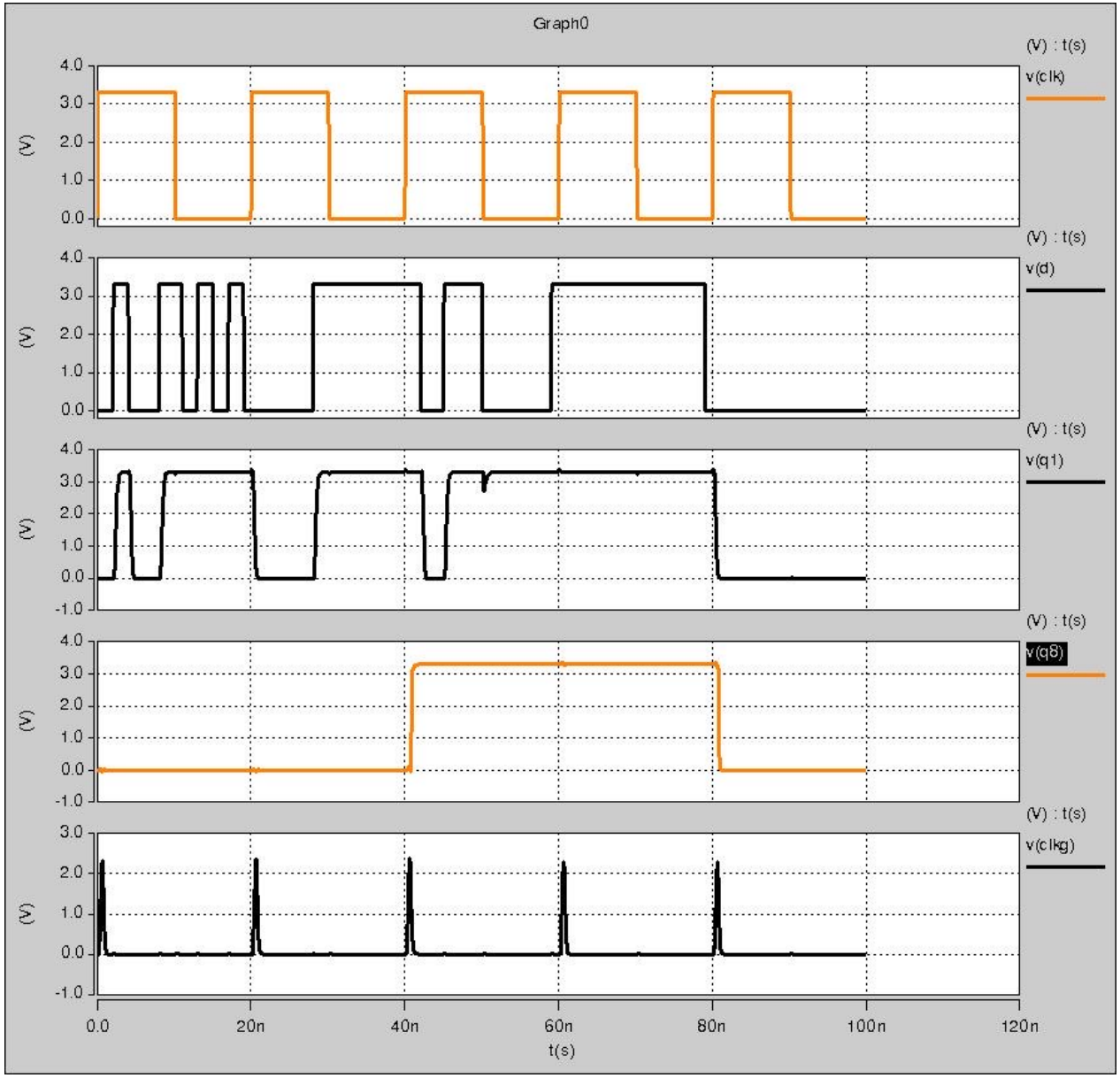
(b) glitch generation



(c) glitch clock

Comparação

```
X1 D q1 clk vcc latch1
X8 D q8 clkg vcc latch1
```



- Mesma latch, transparente no nível alto, controlada por un clock e por um glitch
- **EFEITO**: quando controlada por glitch atua como mestre escravo
- Razão: tempo que a latch fica transparente é muito curto, não ocorredo “race”
- Menor carga na linha do clock

Pulsed Latches

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7 :

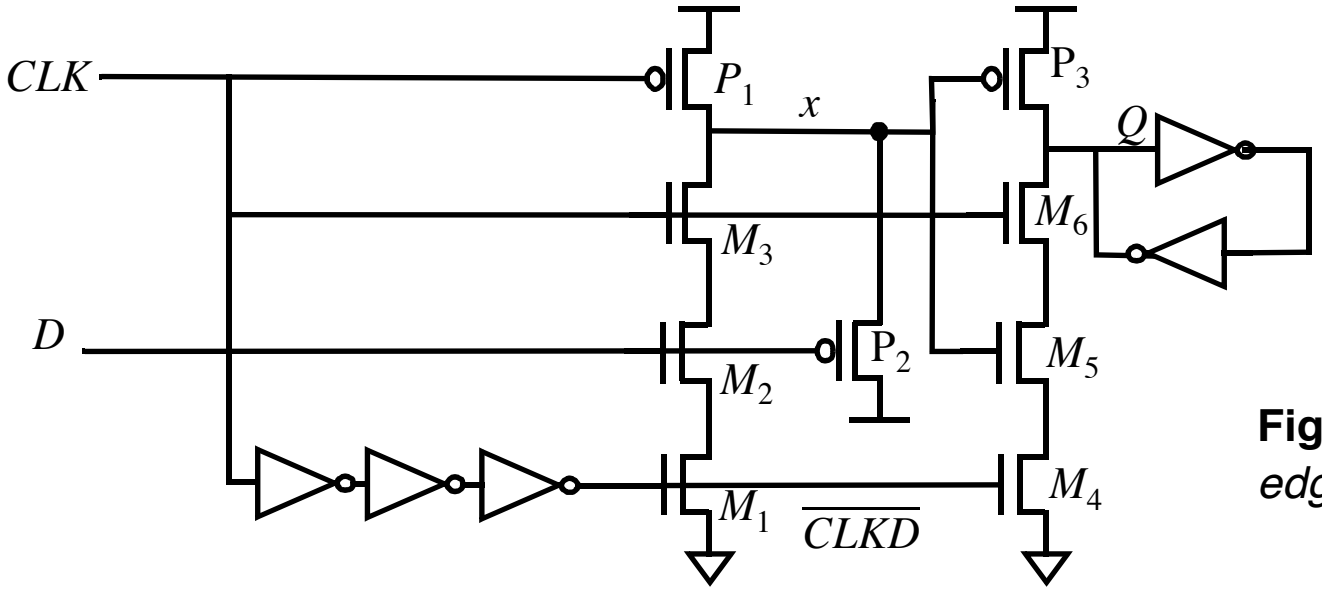
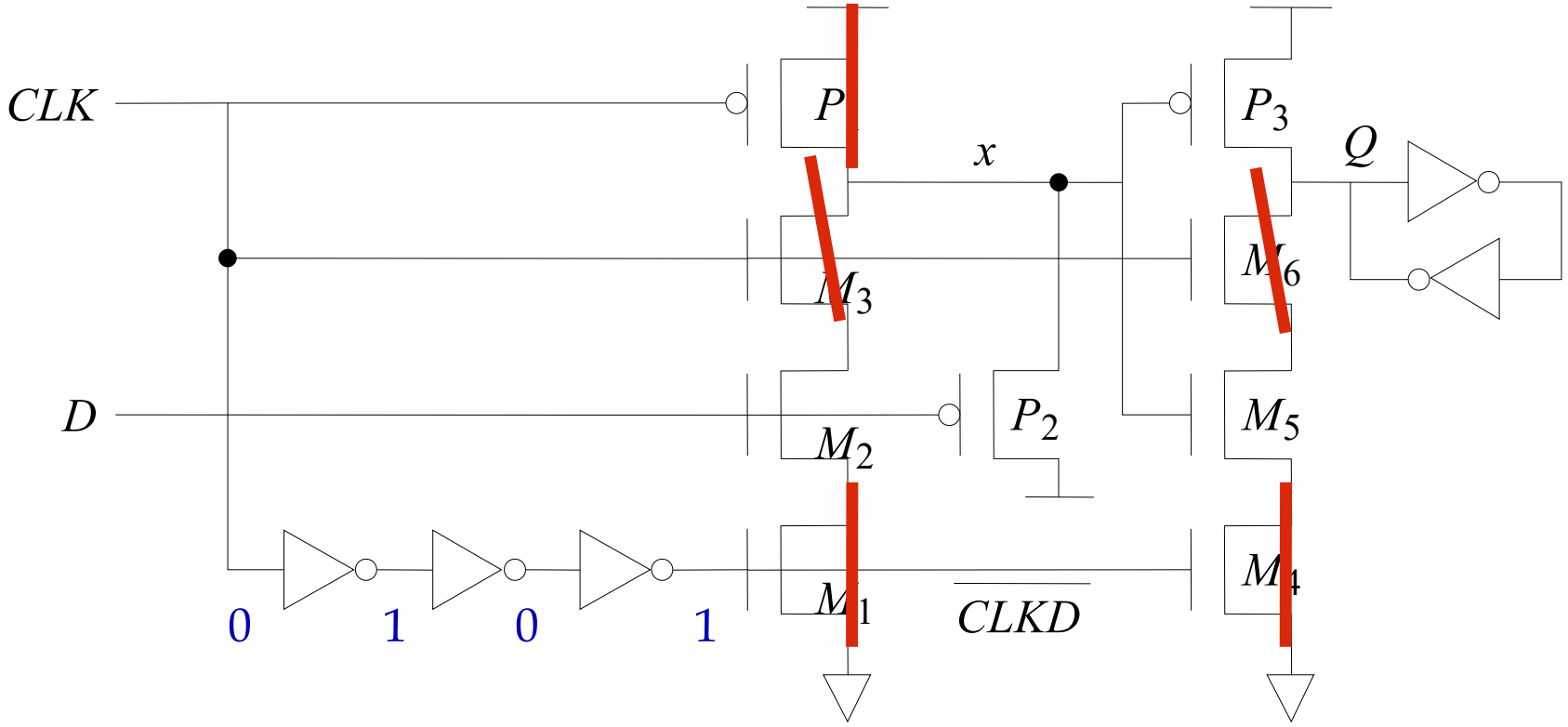


Figure 7.36 Flow-through *positive edge-triggered* register.

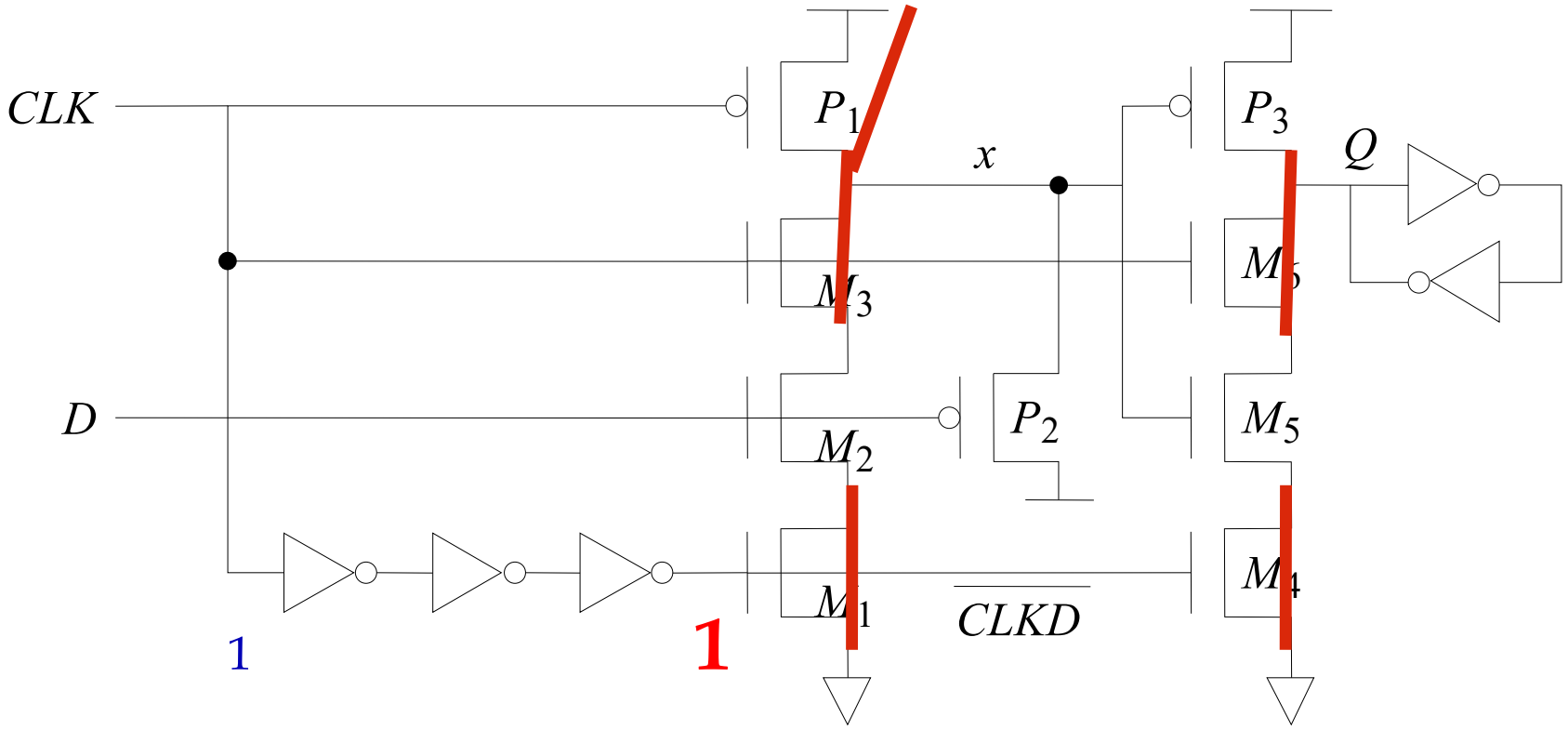
Clock = 0

X em pré-carga 1 (notar P2, não incomoda pois se conduzir leva x a 1)
Saída Q mantém o estado



Clock sobe
por um curto tempo clk=1 e clkd=1

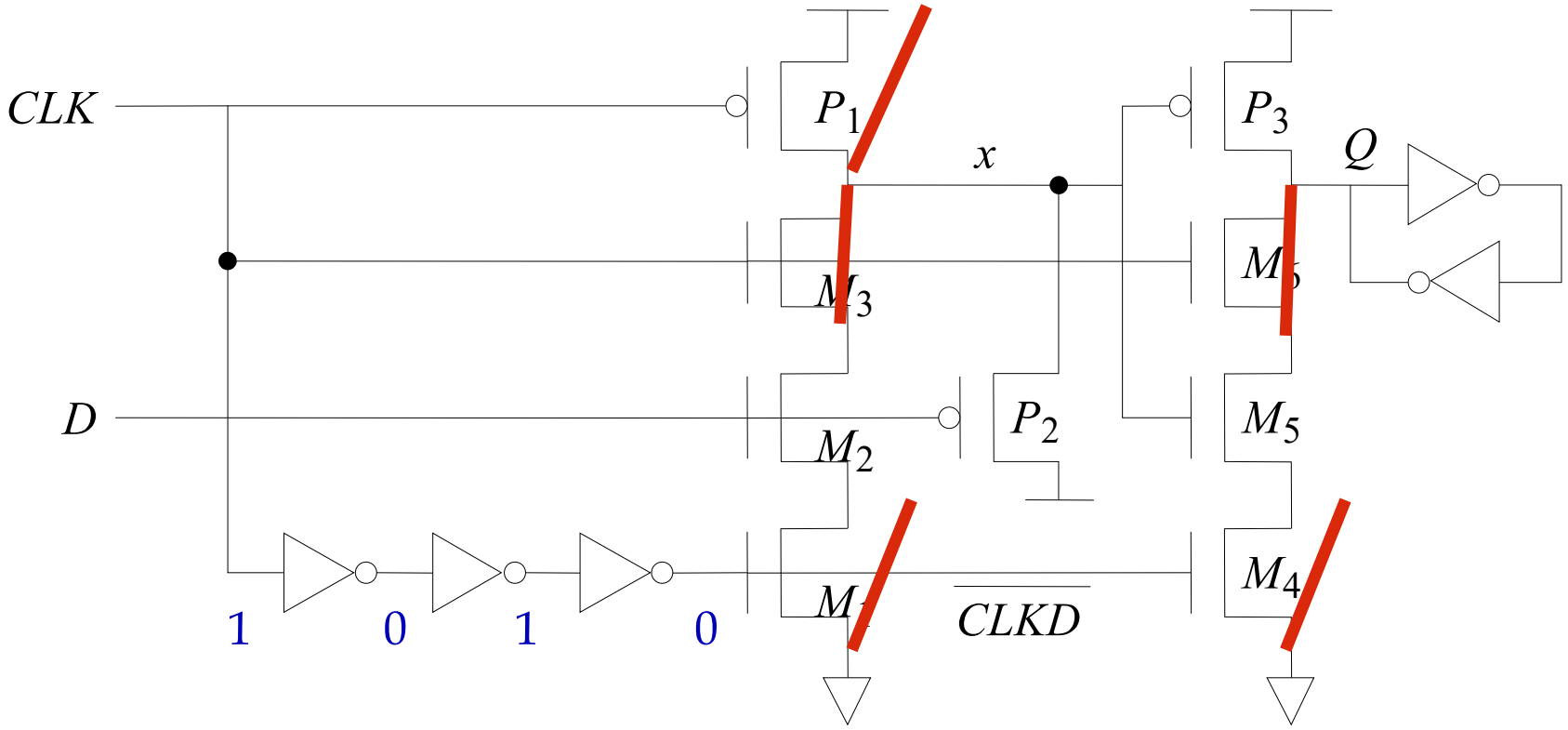
Se D=1 descarrega x, se d=0 x=1. Na prática P2-M2 é um inversor de D.
Par P3-M5 atuam com inversor, e forçam estado de x no par de inversores



Clock = 1

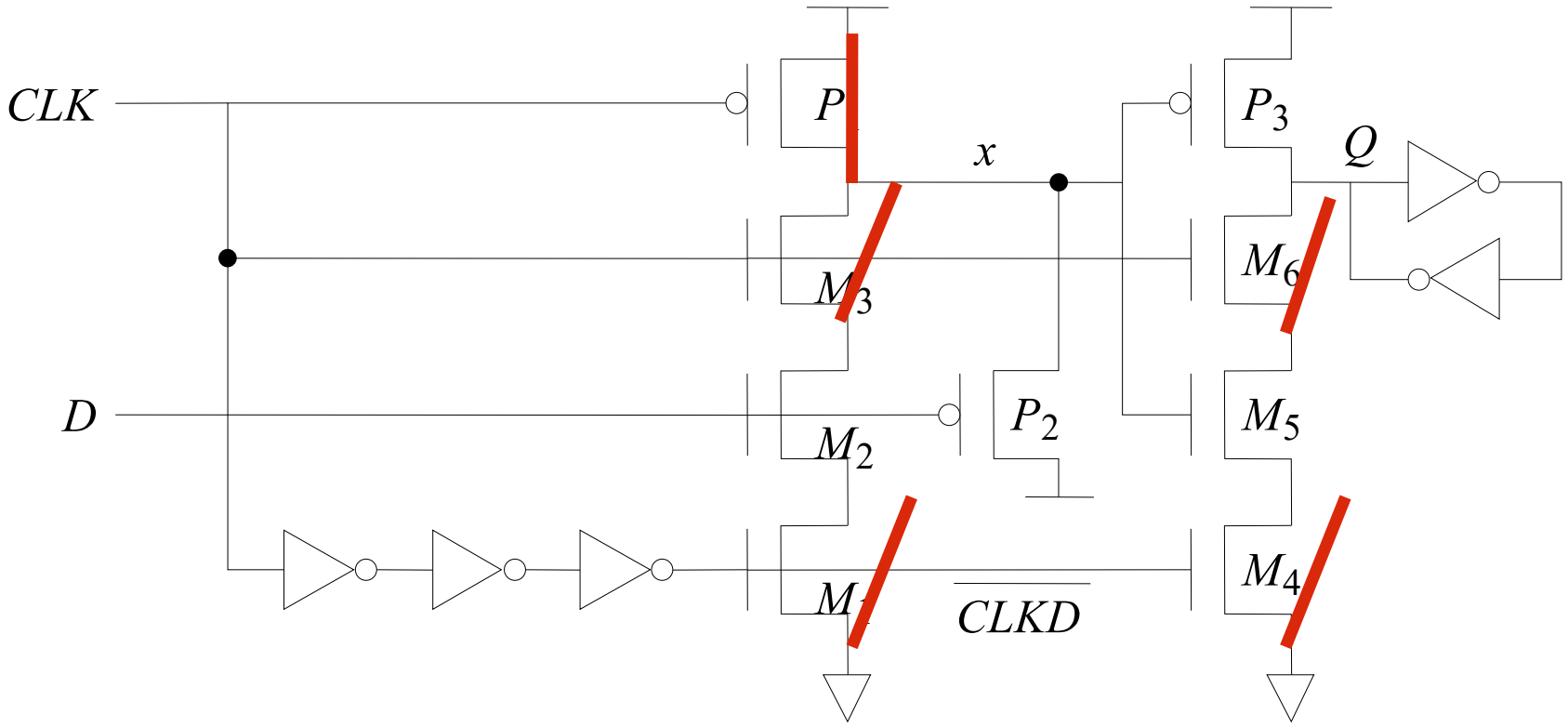
Se D=0 x←1, não faz P3 conduzir
Se D=1 não altera o estado de x

Mantém o estado

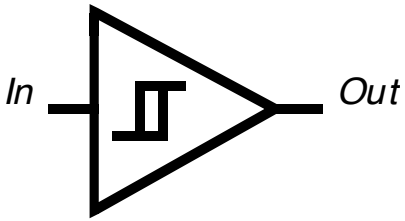


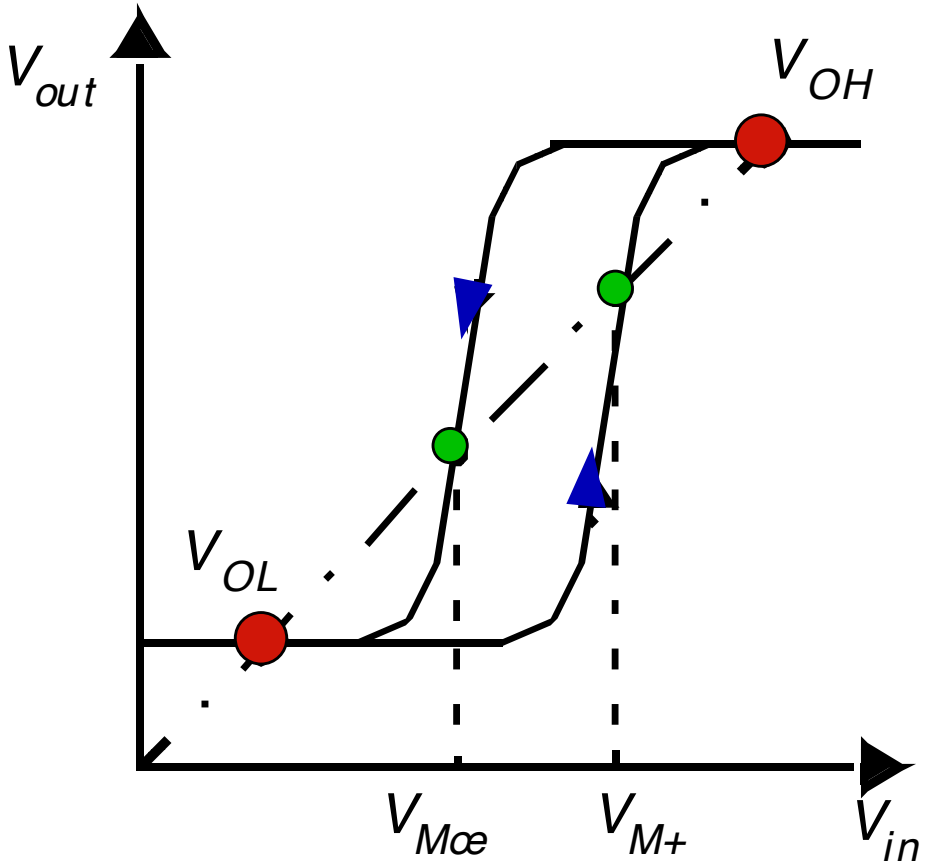
Clock desce
clk e clkd iguais a zero (glitch)

Se D=0 x←1, não faz P3 conduzir
Se D=1 não altera o estado de x



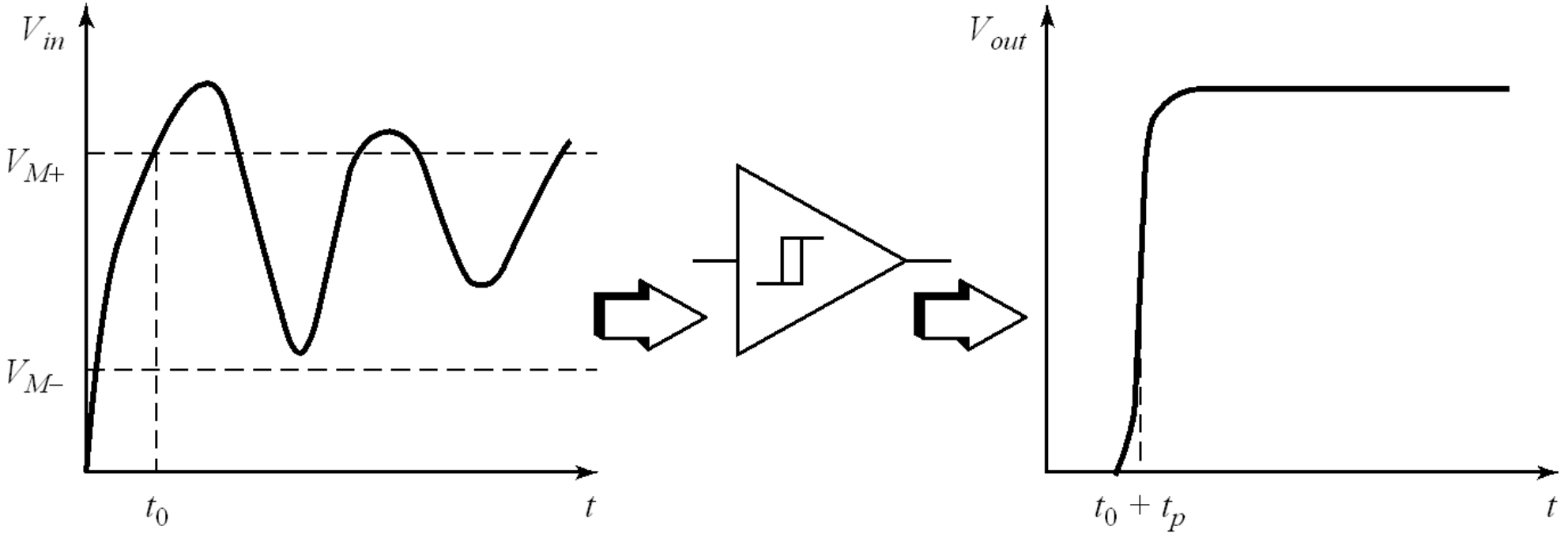
Non-Bistable Sequential Circuits
Schmitt Trigger



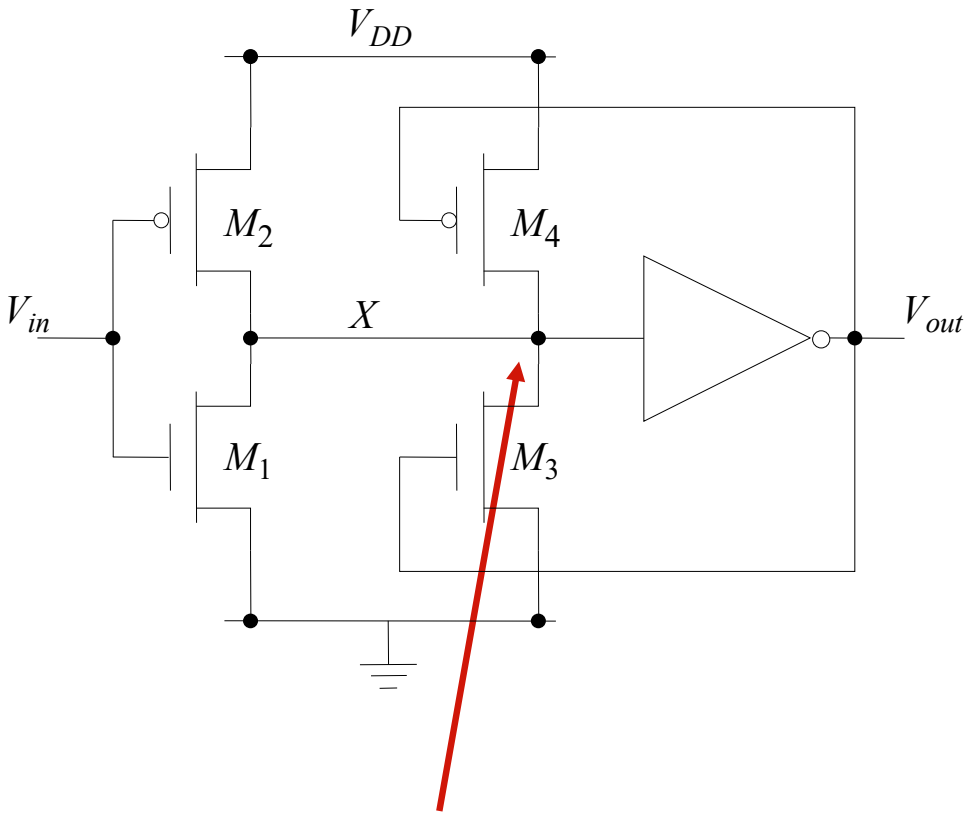


- VTC with hysteresis
- Restores signal slopes

Noise Suppression using Schmitt Trigger



CMOS Schmitt Trigger

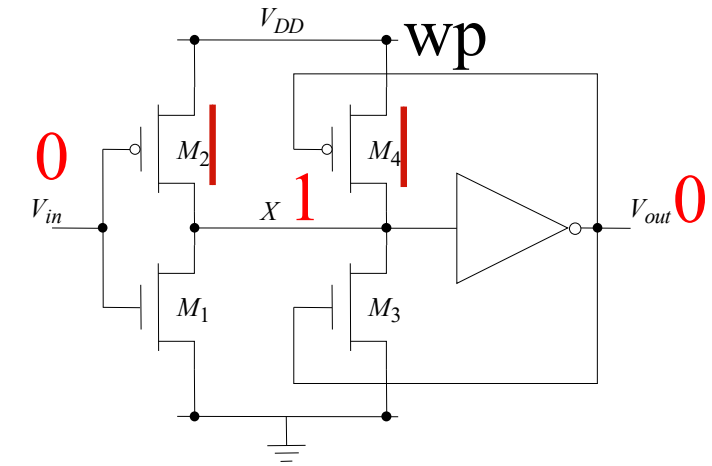


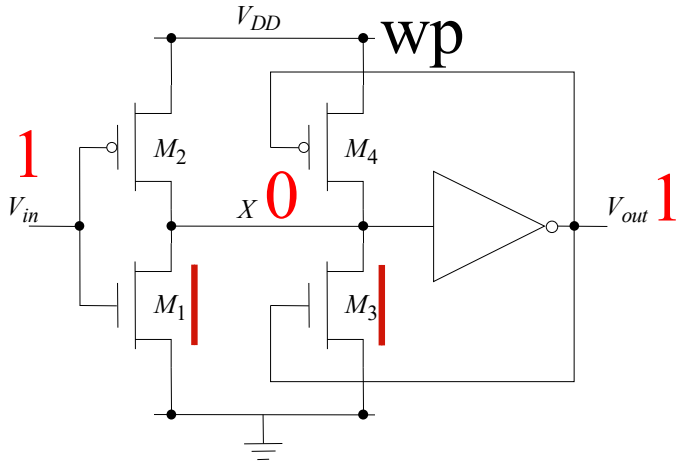

```
.subckt inv in out vcc
MP1   out in vcc vcc pmos l=0.35U W=5.5U
MN2   out in 0   0   nmos l=0.35U W=2.0U
.ends inv

.subckt SCHMITTTRIGGER in out vcc
X1 in X      vcc inv
X2 X out     vcc inv
MP2 X  out vcc vcc pmos l=0.35U W=4U
MN2 X  out   0 0   nmos l=0.35U W=2U
.ends SCHMITTTRIGGER
```

Moves switching threshold of the first inverter

Opera de 2u a 5.5u – mais que 6 microns muito ganho no P e fica em 0

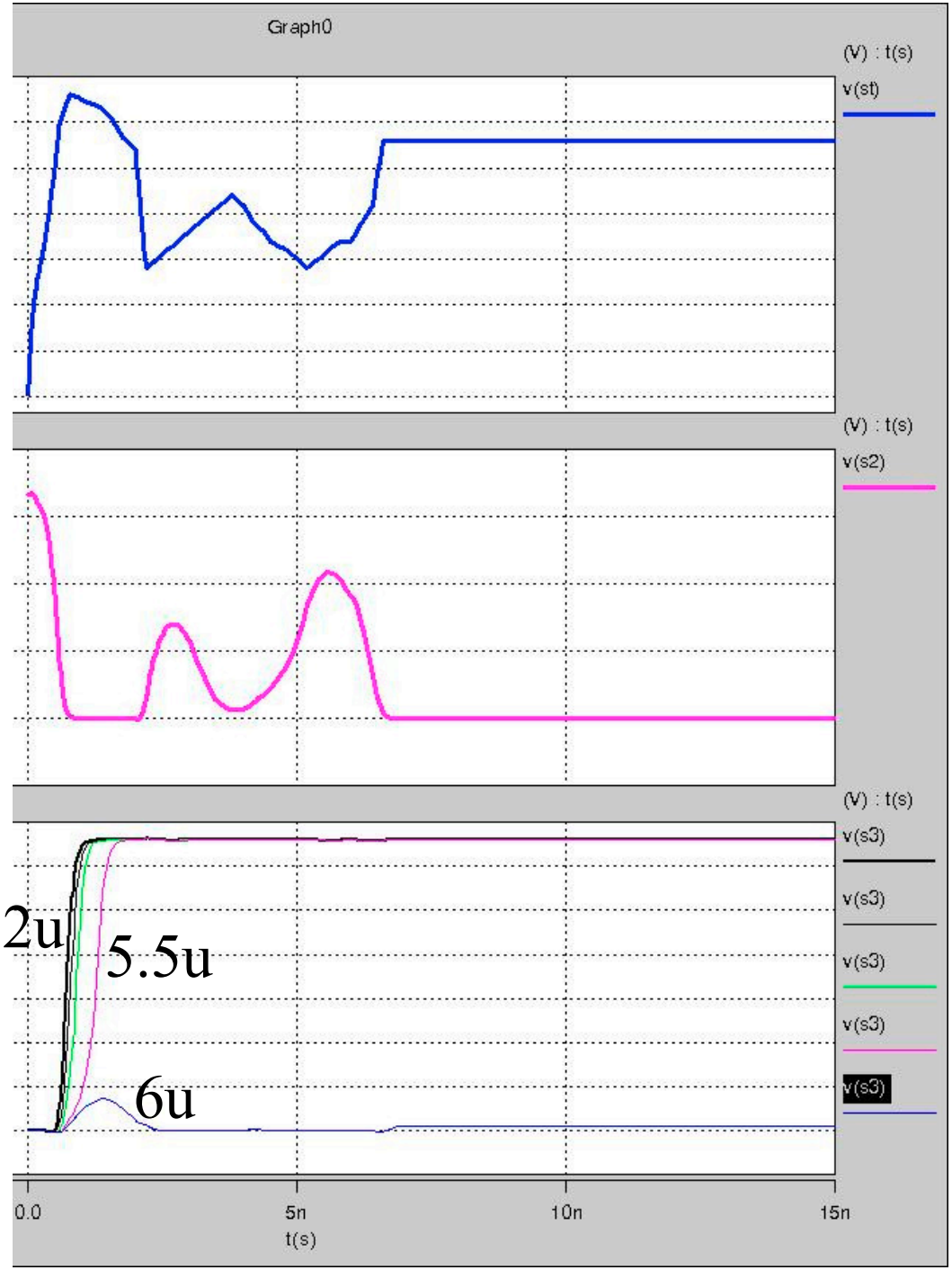




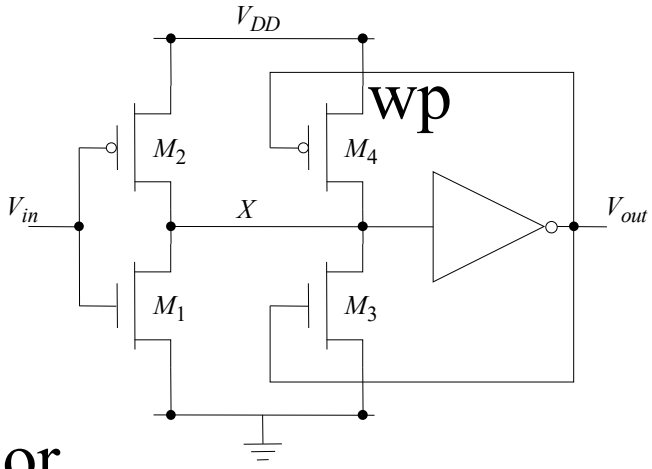
Para passar de 0 para 1:

W(M2) > W(M4)

Se ganho de M4 for maior que o ganho de M2 a saída fica presa em 0



Entrada

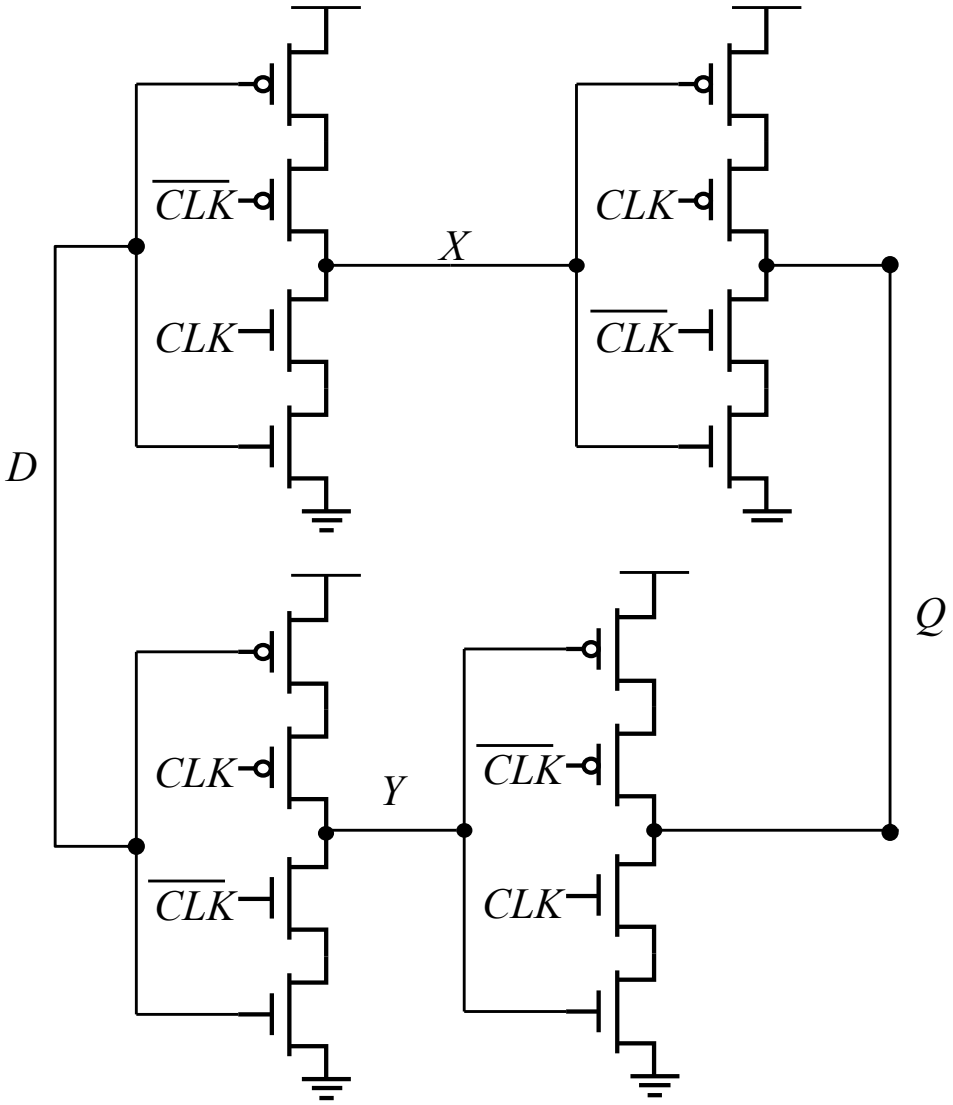


1 inversor

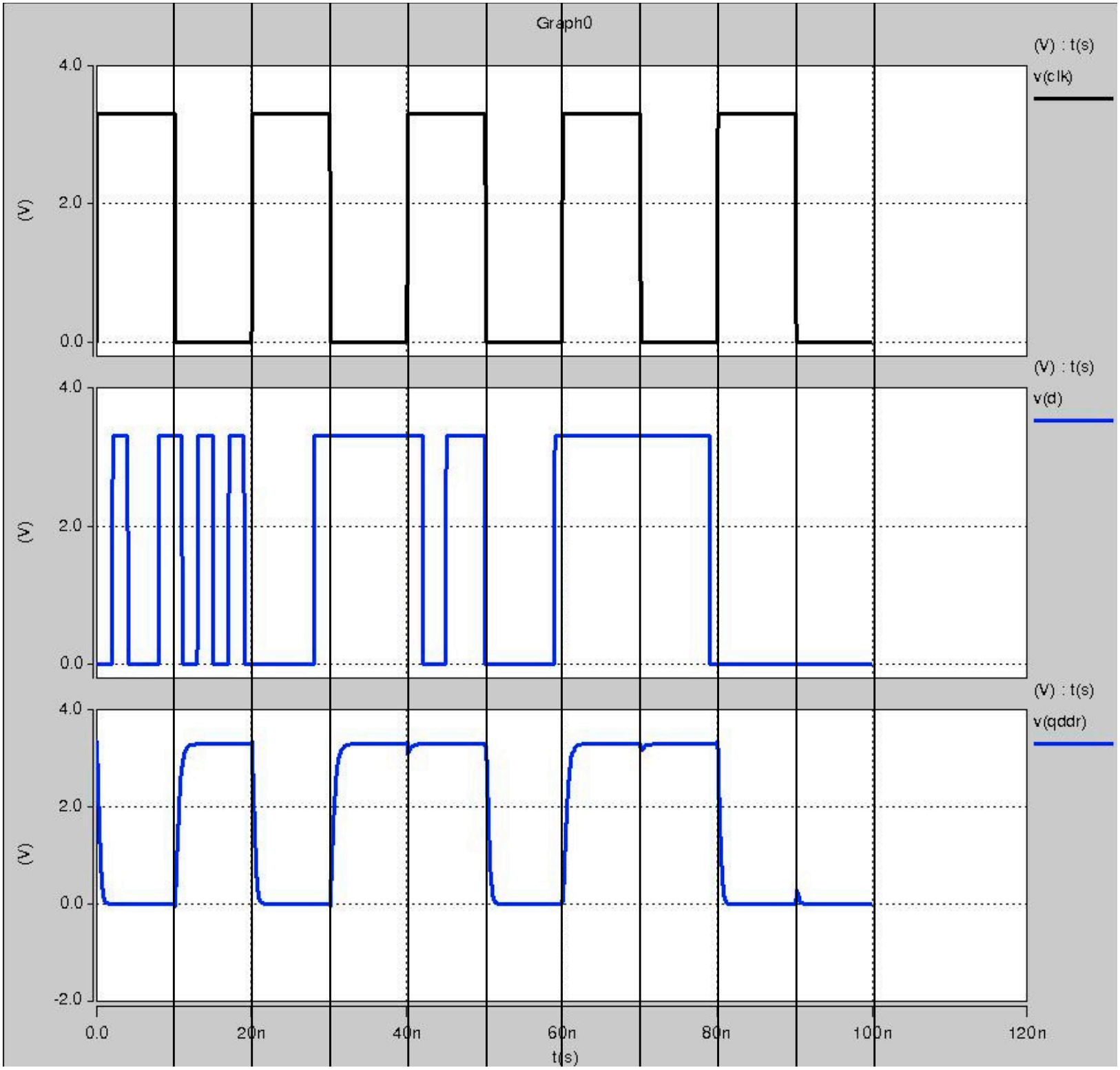
Schmitt Trigger
Parâmetro que varia: wp

Dual – edge flip flop (dinâmico)

- Dual-edge triggered storage element is an edge-sensitive element that captures the value of the input after both low-to-high and high-to-low clock transitions.



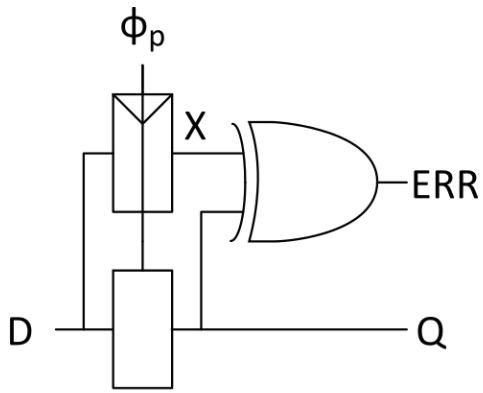
Analisar o circuito ao lado


Graph0
(V) : t(s)
v(clk)
(V) : t(s)
v(d)
(V) : t(s)
v(qddr)
(V)
4.0
2.0
0.0
-2.0
0.0
20n
40n
60n
80n
100n
120n
t(s)

Razor

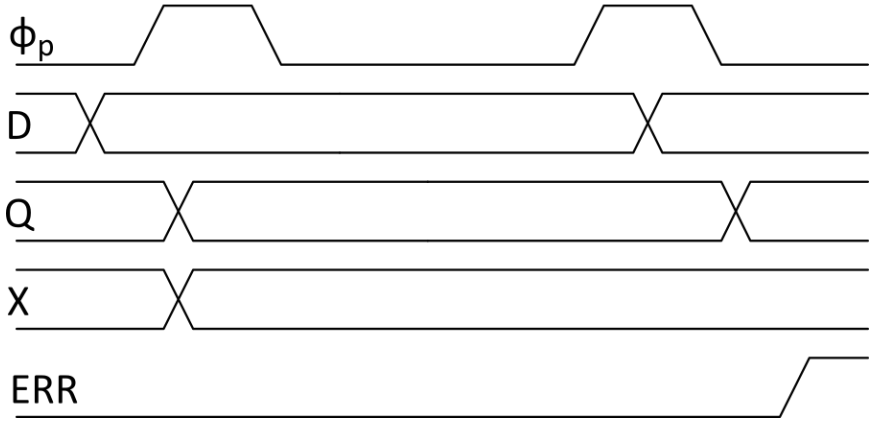
Os projetistas devem incluir margem de tempo na frequência devido:

- tensão
- temperatura
- variação do processo
- dependência de dados
- imprecisões das ferramentas



Alternativa:

- utilizar frequência mais alta e verificar erros falhas
- técnica: ***razor***
- pode reduzir o tempo o período em ~30%

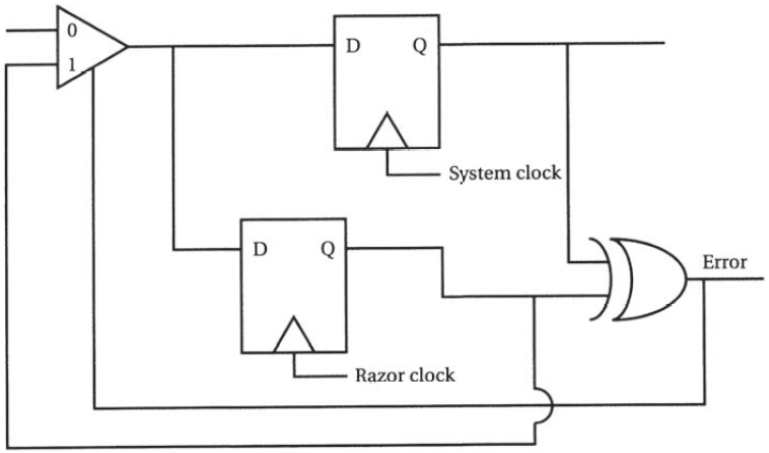


Razor (ENADE)

QUESTÃO 43

O razor é uma arquitetura para desempenho better-than-worst-case que usa um registrador especializado, mostrado na figura, que mede e avalia os erros.

O registrador do sistema mantém o valor chaveado e é comandado por um *clock* de sistema *better-than-worst-case*. Um registrador adicional é comandado separadamente por um *clock* ligeiramente atrasado com relação ao do sistema. Se os resultados armazenados nos dois registradores são diferentes, então um erro ocorreu, provavelmente devido a temporização. A porta XOR detecta o erro e faz com que esse valor seja substituído por aquele do registrador do sistema.



Considerando essas informações, analise as afirmações a seguir.

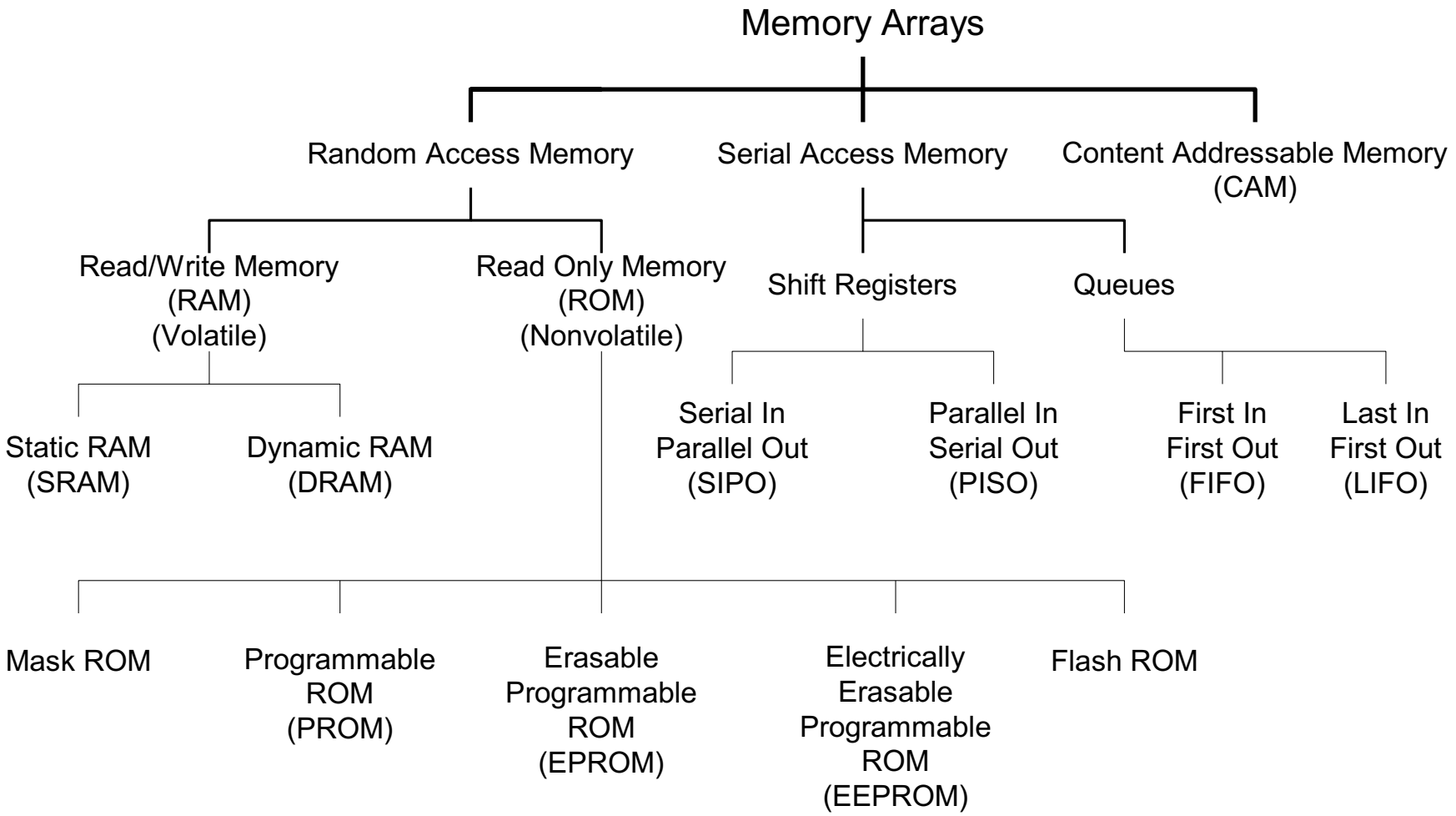
I. Sistemas digitais são tradicionalmente concebidos como sistemas assíncronos regidos por um clock.

II. Better-than-worst-case é um estilo de projeto alternativo em que a lógica detecta e se recupera de erros, permitindo que o circuito possa operar com uma frequência maior.

III. Nos sistemas digitais, o período de clock é determinado por uma análise cuidadosa para que os valores sejam armazenados corretamente nos registradores, com o período de clock alargado para abranger o atraso de pior caso.

Quais são corretas? Por quê?

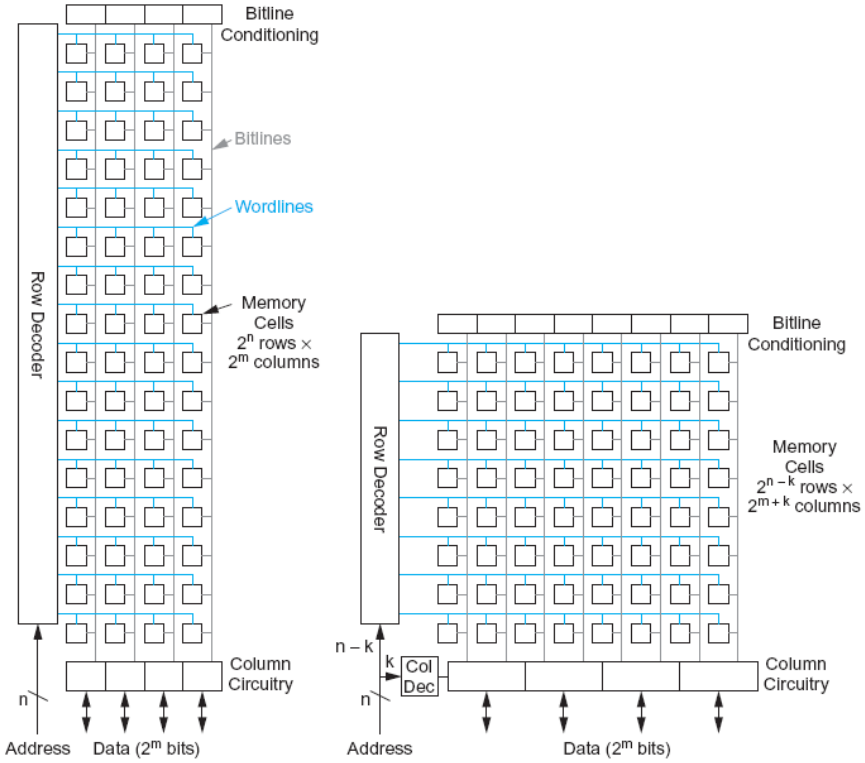
Memórias



Fonte: ARM

Array Architecture

- 2^n *words* of 2^m *bits* each
- If n >> m, fold by 2^k into fewer *rows* of more *columns*

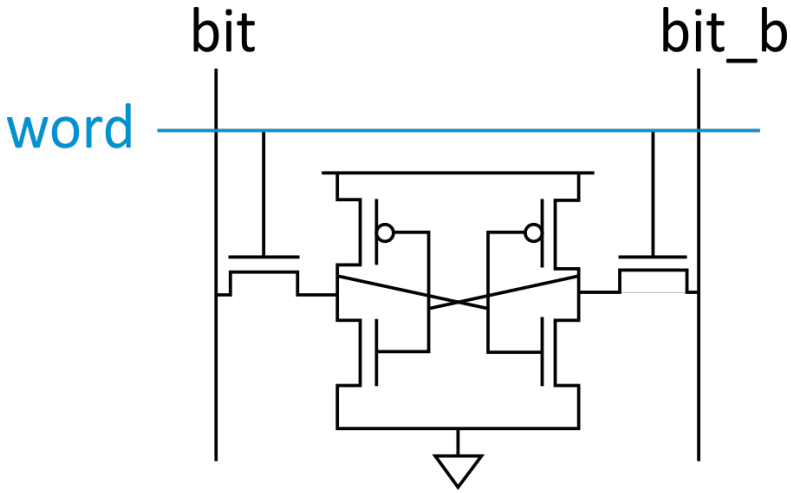


- Good regularity – easy to design
- Very high density if good cells are used

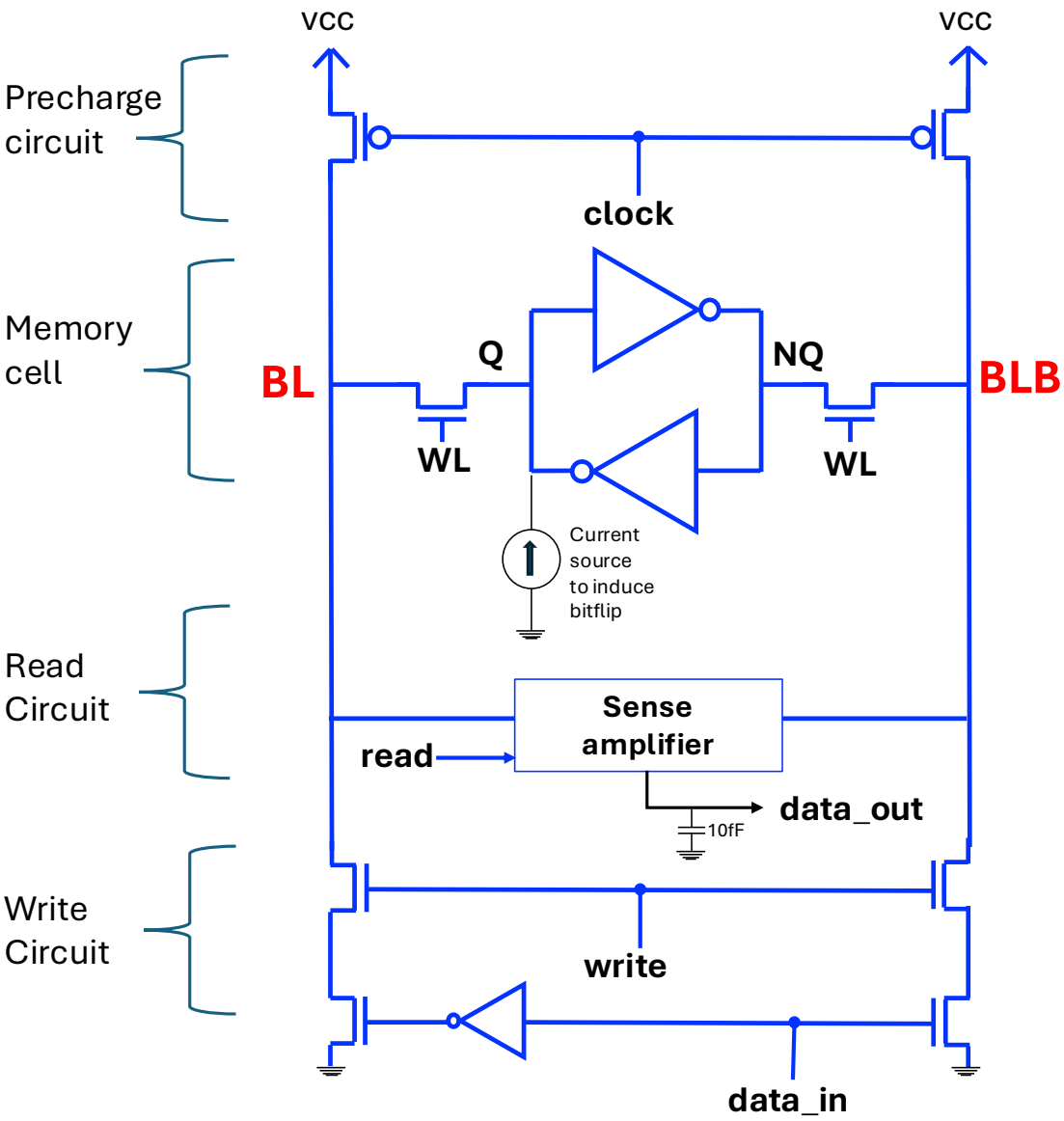
Fonte: ARM

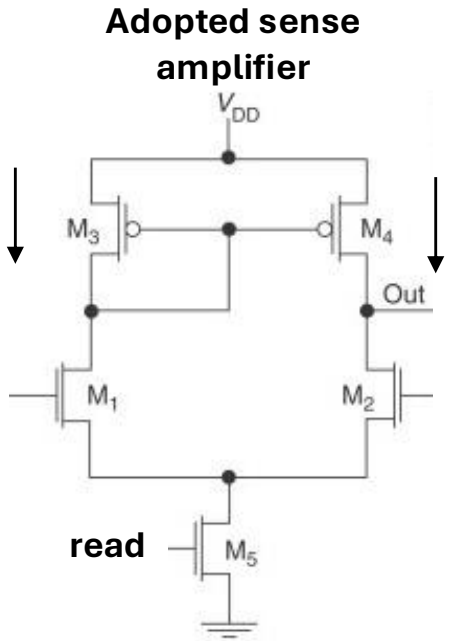
6T SRAM Cell

- Cell size accounts for most of array size
  - Reduce cell size at expense of complexity
- 6T SRAM Cell
  - Used in most commercial chips
  - Data stored in cross-coupled inverters
- Read:
  - Precharge bit, bit_b
  - Raise wordline
- Write:
  - Drive data onto bit, bit_b
  - Raise wordline

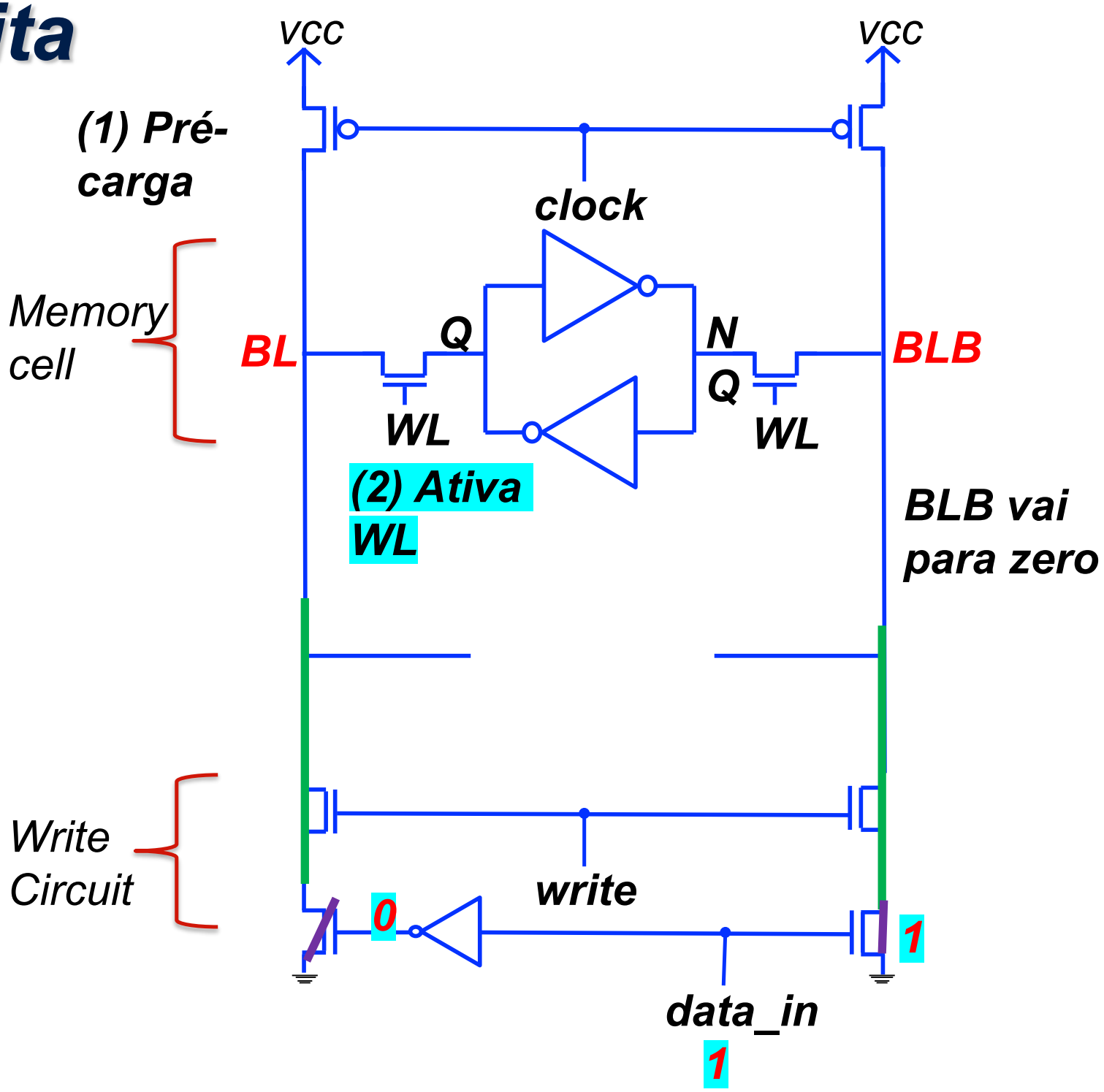


Fonte: ARM

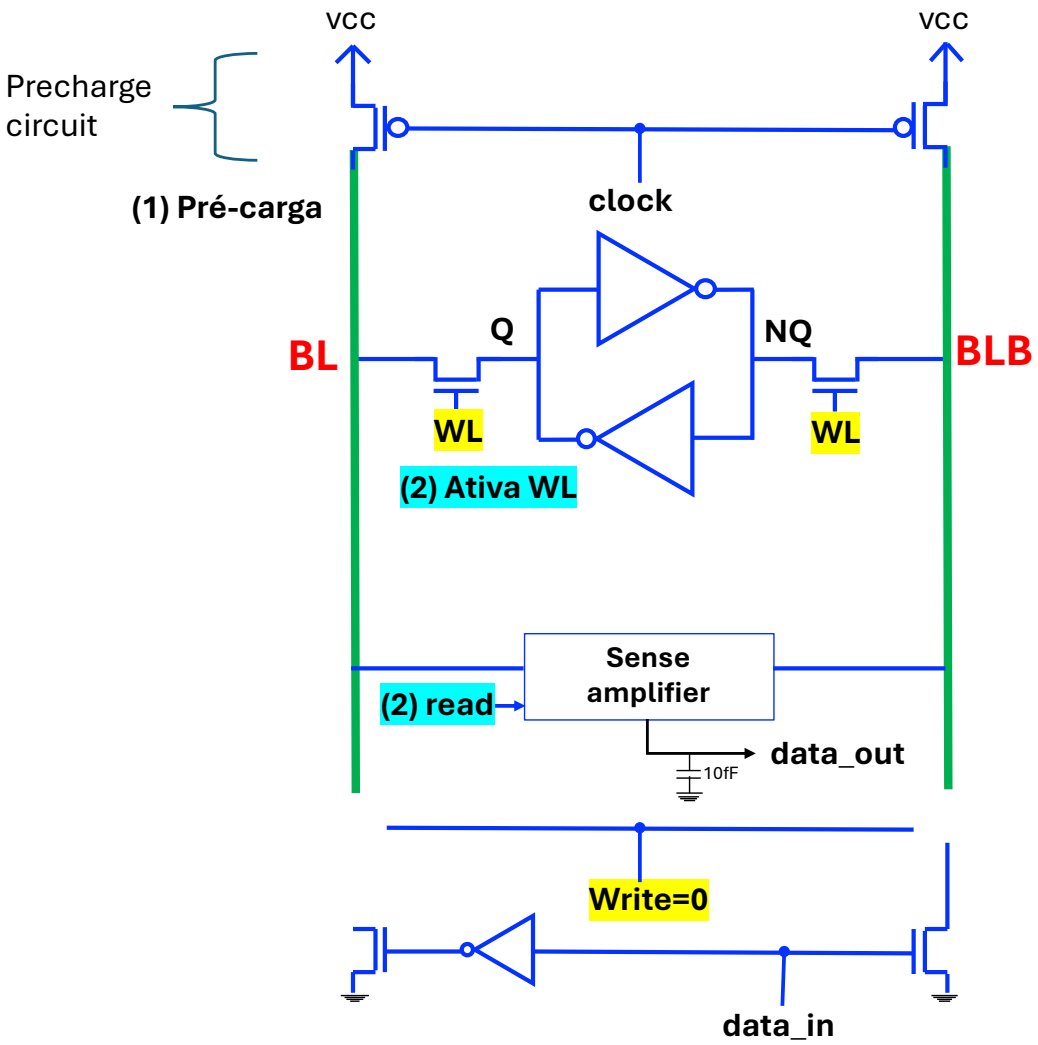

Precharge circuit
Memory cell
Read Circuit
Write Circuit
VCC
VCC
clock
BL
Q
NQ
BLB
WL
WL
Current source to induce bitflip
Sense amplifier
read
data_out
10fF
write
data_in


Adopted sense amplifier
V_{DD}
M_3
M_4
Out
M_1
M_2
read
M_5

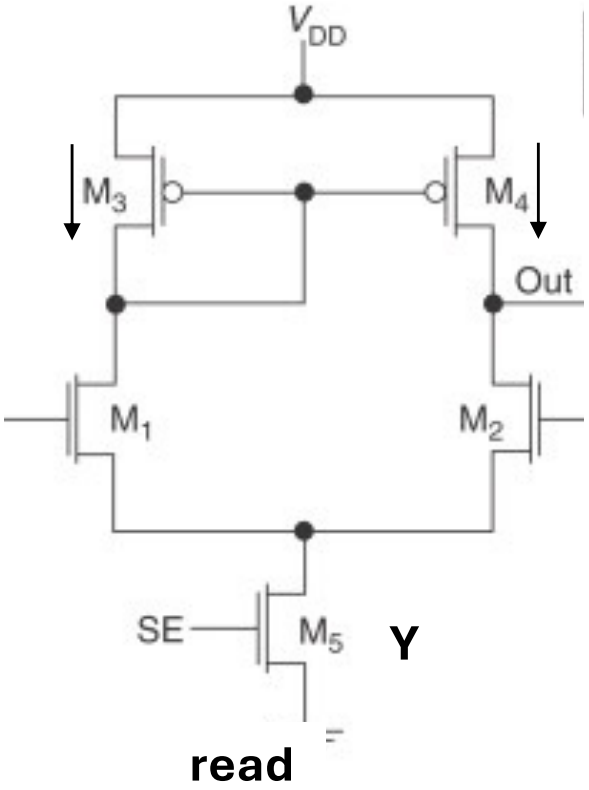
Escrita


(1) Pré-carga
Memory cell
Write Circuit
VCC
VCC
clock
BL
Q
N
Q
BLB
WL
WL
(2) Ativa WL
BLB vai para zero
write
0
1
data_in
1

Leitura Diferencial



I(M3)=I(M4)



M_3 e M_4: PMOS formam um **espelho de corrente**.
M_3 é o transistor de referência e M_4 copia a corrente.

→ **Durante a pré-carga: M1 e M2 conduzindo e Y devido a M5 aberto ~1**

→ **Na leitura**

➔ se M1 (BL=1) fecha os P conduzem e saída vai para para 1

➔ se M2 (BLB=1) fecha saída vai para zero