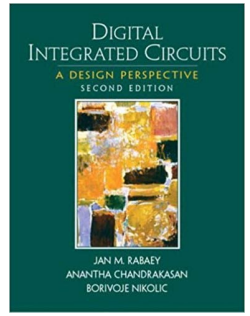
Microeletrônica

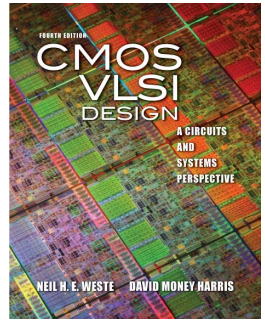
Aula #2 → Inversor - comportamento estático e dinâmico

- Professor: Fernando Gehm Moraes
- Livro texto:

  Digital Integrated Circuits a Design Perspective - Rabaey

  C MOS VLSI Design - Weste





Revisão das lâminas: 07/março/2025

Inversor

Portas Lógicas Digitais: Parâmetros Fundamentais

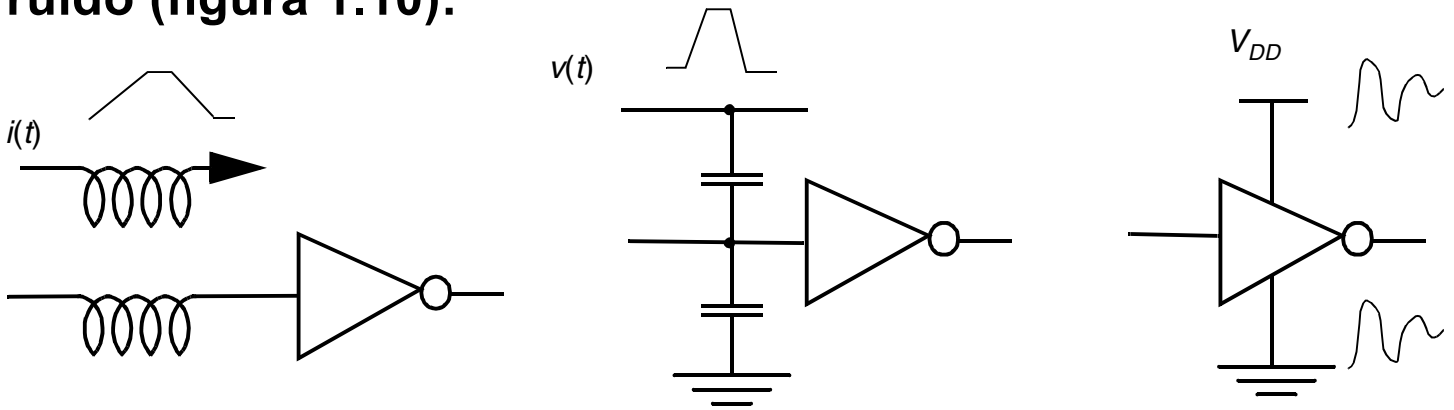
- Funcionalidade
- PPA
  - **P**ower
  - **P**erformance
  - **A**rea
- Energia

Inversor

Ruído em Circuitos Integrados Digitais

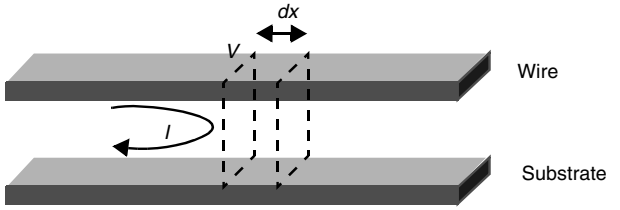
Ruído significa variação indesejada de tensão ou de corrente nos nós lógicos

Fontes de ruído (figura 1.10):



Acoplamento Indutivo | Acoplamento Capacitivo | Ruído de Alimentação

Most noise in a digital system is internally generated, and the noise value is proportional to the signal swing. Capacitive and inductive cross talk, and the internally-generated power supply noise are examples of such. Other noise sources such as input power supply noise are external to the system, and their value is not related to the signal levels. For these sources, the noise level is directly expressed in Volt or Ampere. Noise sources that are a function of the signal level are better expressed as a fraction or percentage of the signal level. Noise is a major concern in the engineering of digital circuits. How to cope with all these disturbances is one of the main challenges in the design of high-performance digital circuits and is a recurring topic in this book.



Inversor

Porta Ideal

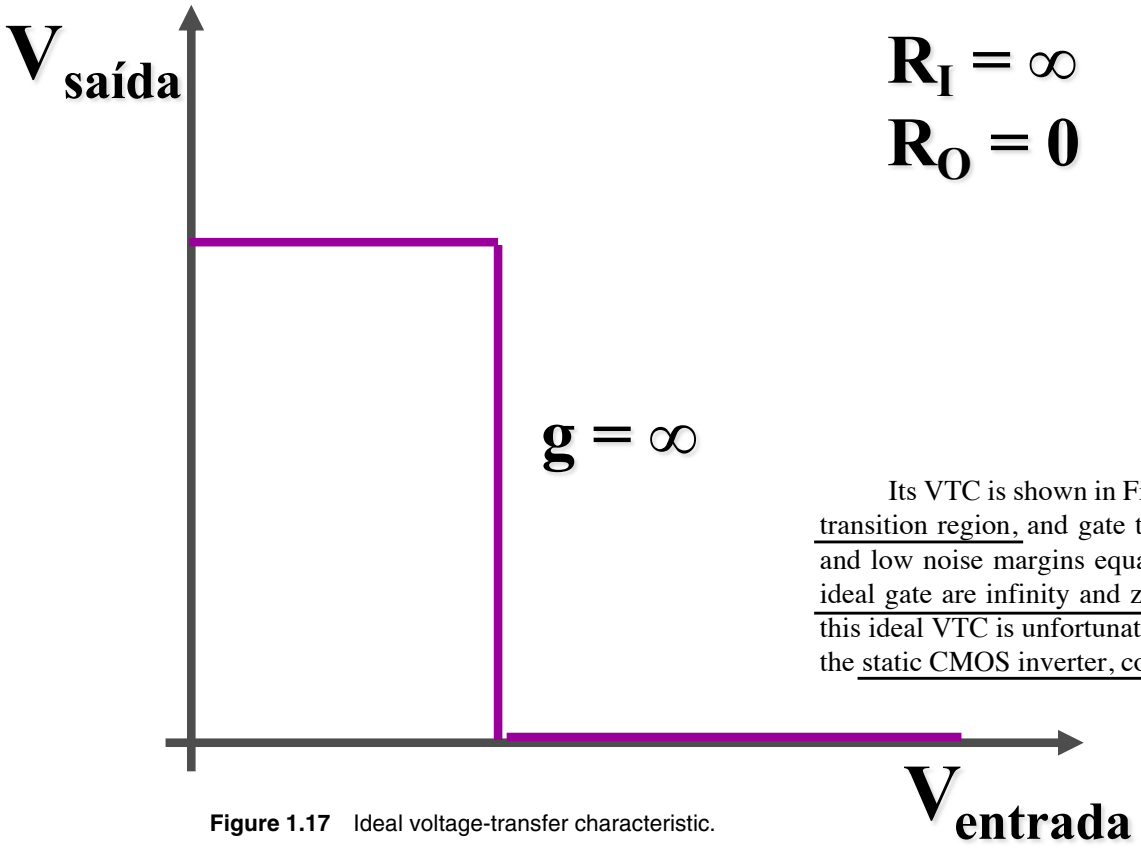
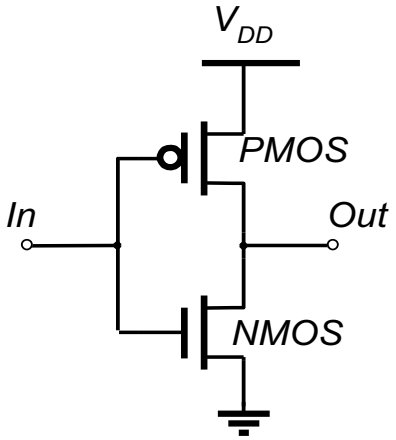


Figure 1.17 Ideal voltage-transfer characteristic.

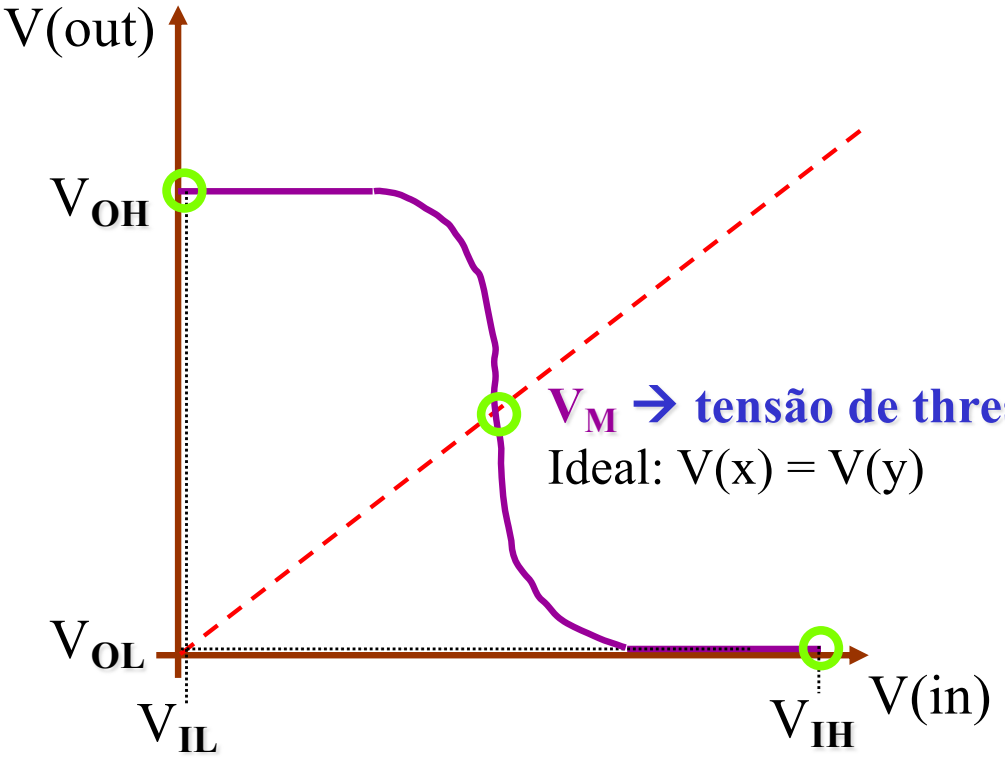
$$R_I = \infty$$
$$R_O = 0$$



Its VTC is shown in Figure 1.17 and has the following properties: infinite gain in the transition region, and gate threshold located in the middle of the logic swing, with high and low noise margins equal to half the swing. The input and output impedances of the ideal gate are infinity and zero, respectively (i.e., the gate has unlimited fan-out). While this ideal VTC is unfortunately impossible in real designs, some implementations, such as the static CMOS inverter, come close.

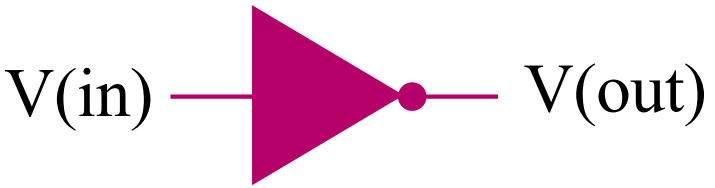
Inversor

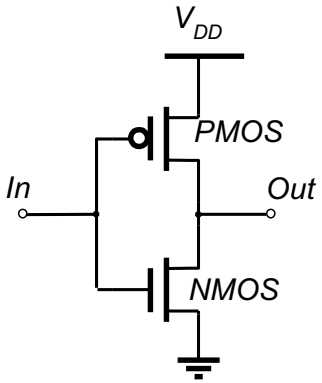
Operação DC: Característica de Transferência de Tensão



V_M → tensão de threshold de chaveamento

Ideal: V(x) = V(y)



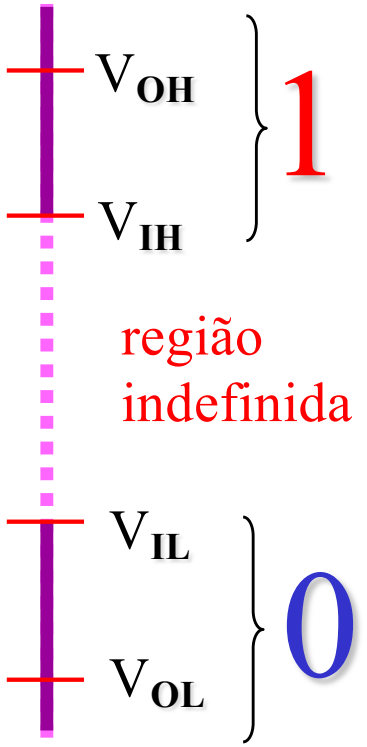


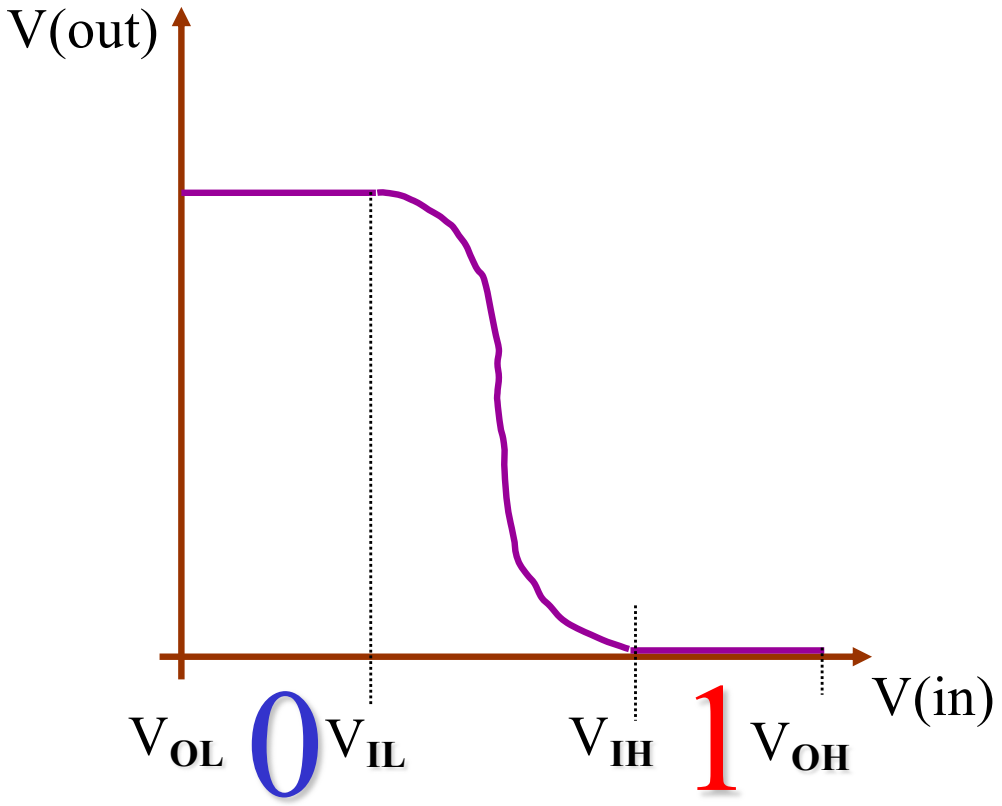
➔ Porque V_M na meia-excursão do tensão de entrada?

OBS: Não V_M confundir com V_T que é a tensão de threshold do transistor

Inversor

Mapeamento entre sinais analógicos e digitais





Quanto maiores as regiões “0” e “1’ maior imunidade ao ruído

Inversor CMOS

Resposta Estática

- **Excursão da saída igual aos valores da alimentação**
- **Os níveis lógicos não dependem do dimensionamento dos transistores**
- **Baixa impedância de saída (< 10 kΩ)** – ideal: zero
- **Altíssima resistência de entrada** – ideal: infinita
- **Curva de transferência de tensão (VTC) simétrica**
- **Tempo de propagação do sinal é função:**
  - **capacitância de carga**
  - **resistência dos transistores**
- **Não há dissipação de potência estática**
- **Caminho de corrente direto durante o chaveamento**

Comportamento DC do inversor CMOS estático

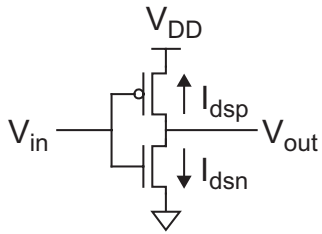


FIGURE 2.25
A CMOS inverter

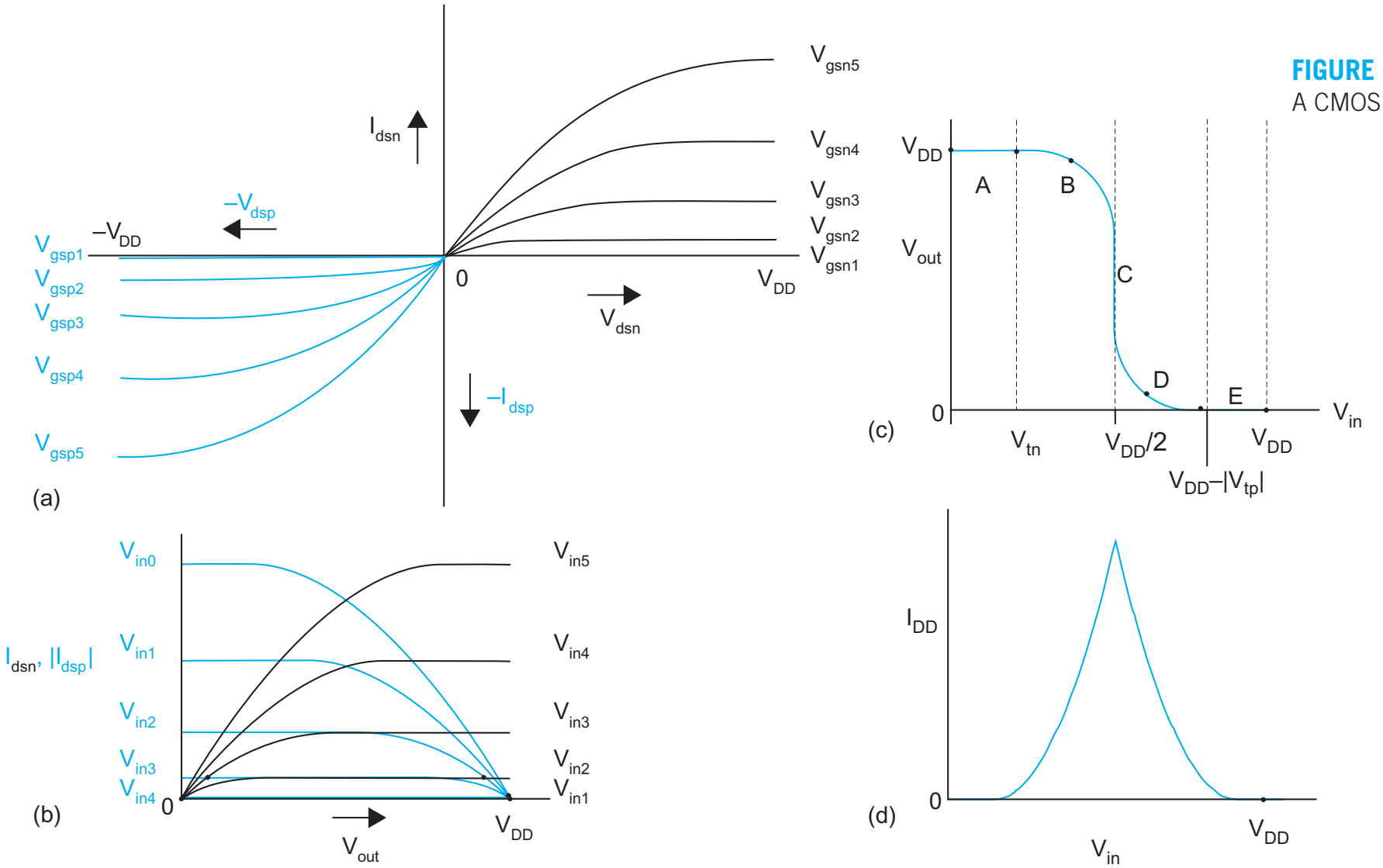


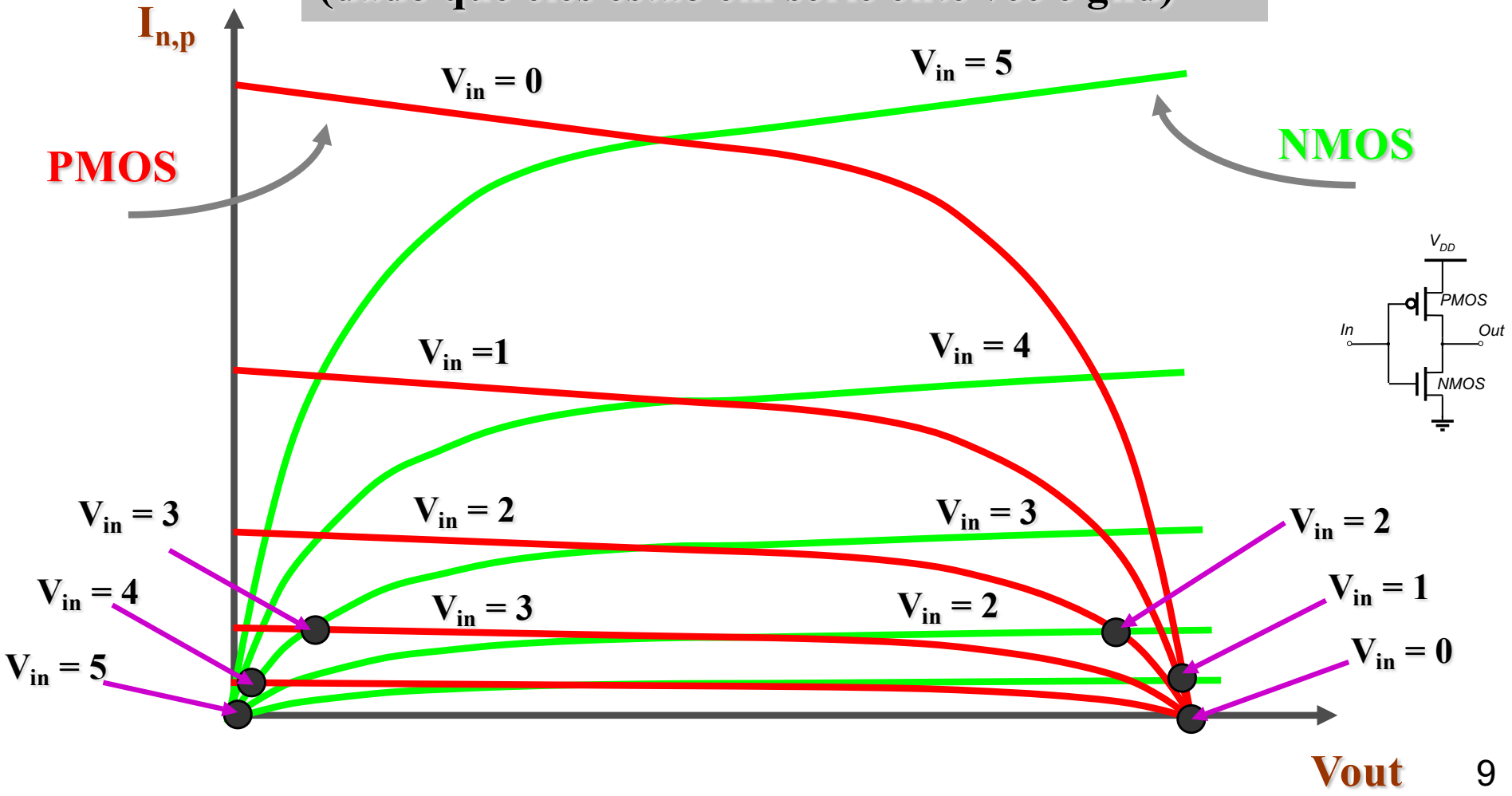
FIGURE 2.26 Graphical derivation of CMOS inverter DC characteristic

Referência: Weste

Inversor CMOS

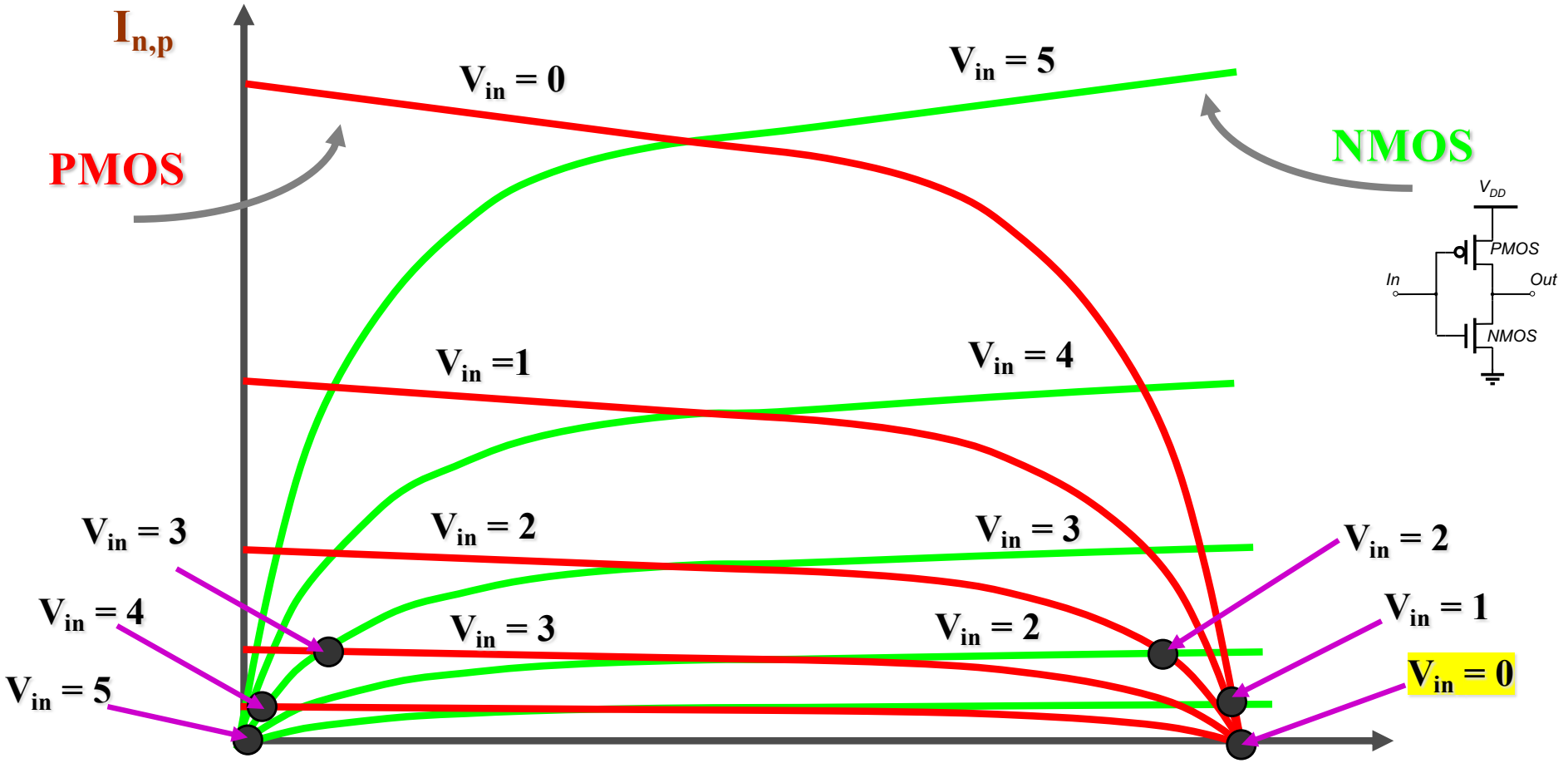
Curva de corrente dos transistores N e P

Pontos válidos In = Ip
(dado que eles estão em série ente vcc e gnd)



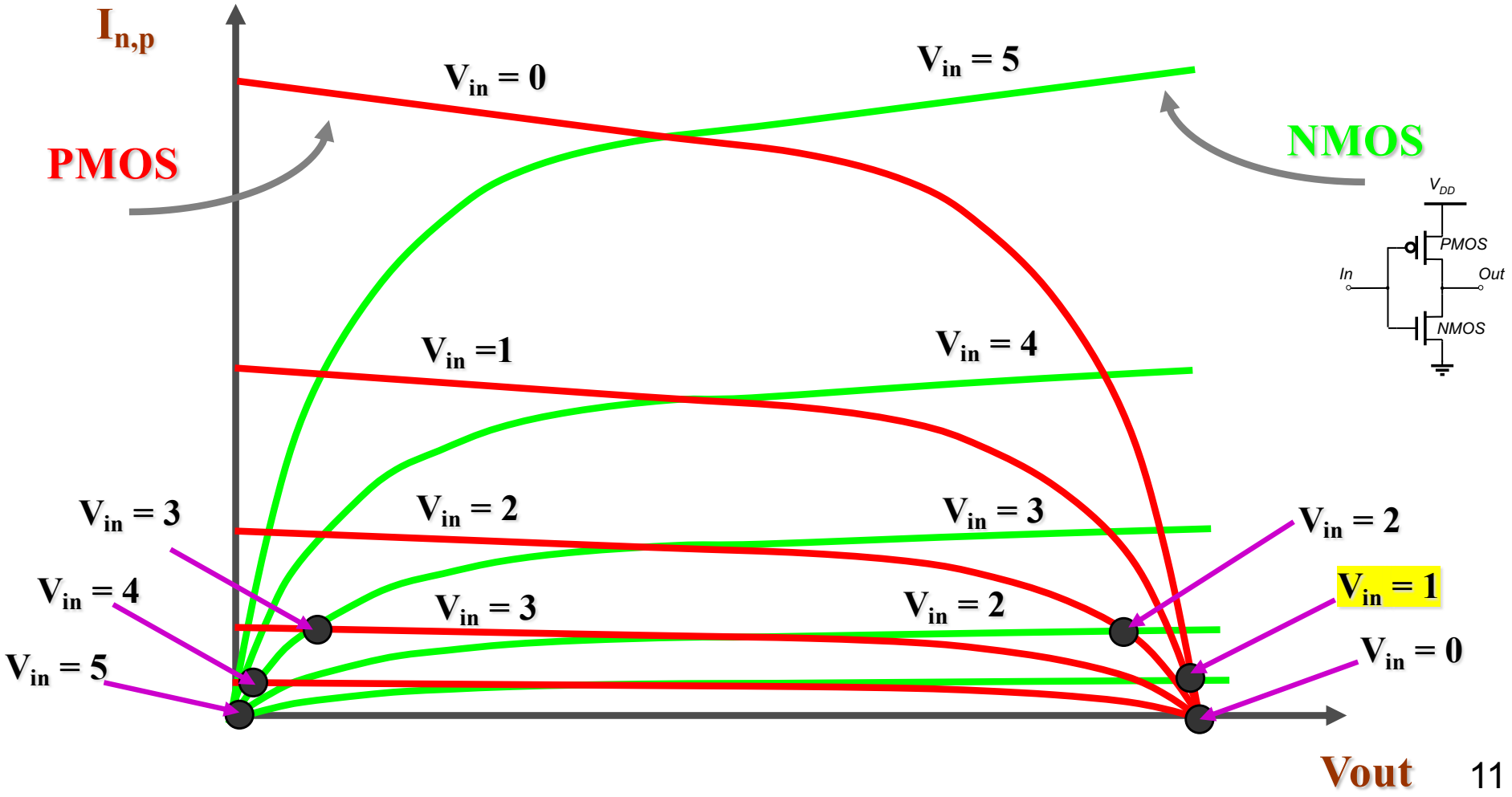
Inversor CMOS

Vin=0:
Saída = Vdd
Transistor N e P com corrente ≈ 0



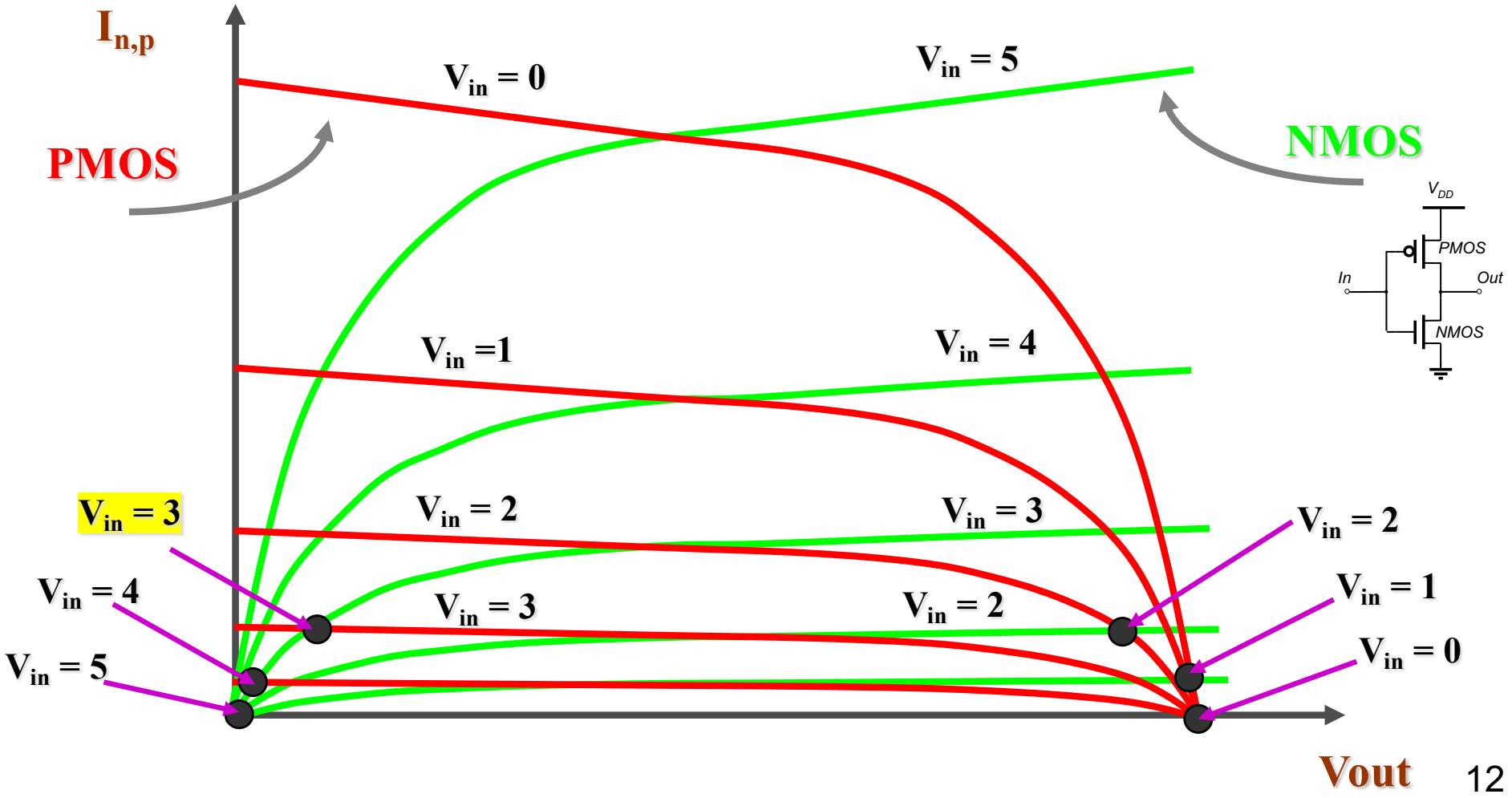
Inversor CMOS

Vin=1:
Saída ainda próxima de Vdd
Início de condução do transistor N



Inversor CMOS

Vin=3:
Passagem abrupta para saída próxima de zero



Inversor CMOS

Curvas de Transferência de Tensão (VTC)

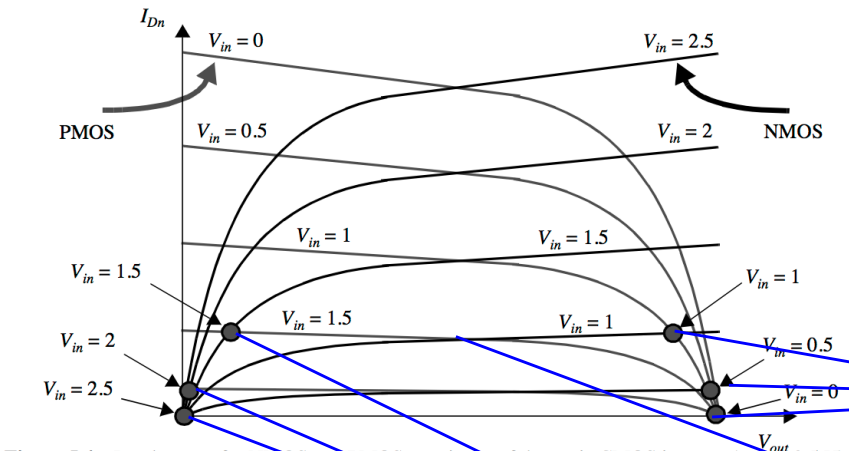
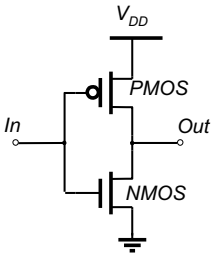


Figure 5.4 Load curves for NMOS and PMOS transistors of the static CMOS inverter (V_{DD} = 2.5 V). The dots represent the dc operation points for various input voltages.



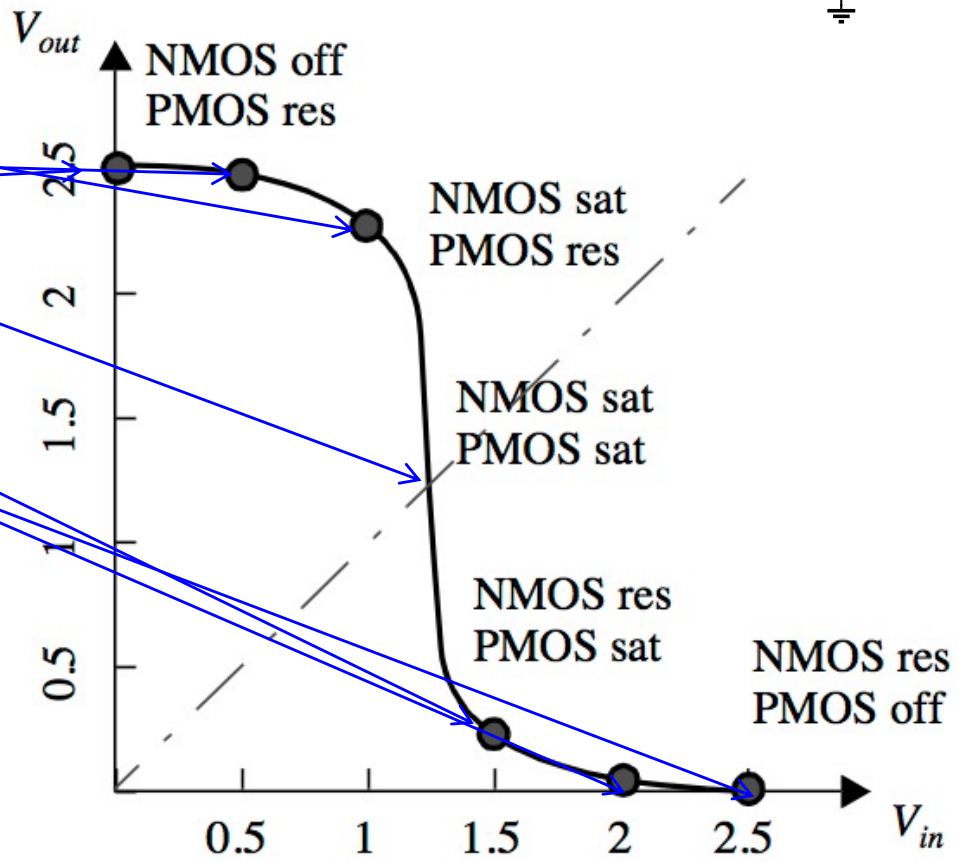
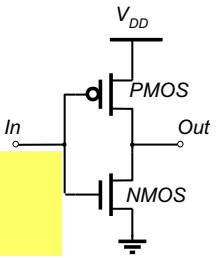


Figure 5.5 VTC of static CMOS inverter, derived from Figure 5.4 (V_{DD} = 2.5 V). For each operation region, the modes of the transistors are annotated — off, res(istive), or sat(urated).

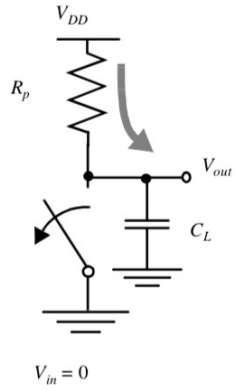
Inversor CMOS

Corrente com carga de saída



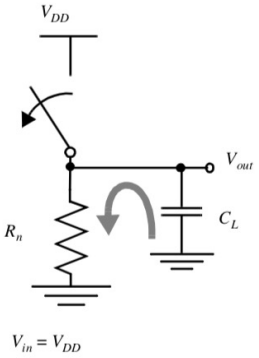
1

Entrada 0 satura o T_P



(a) Low-to-high

Entrada 1 satura o T_n



(b) High-to-low

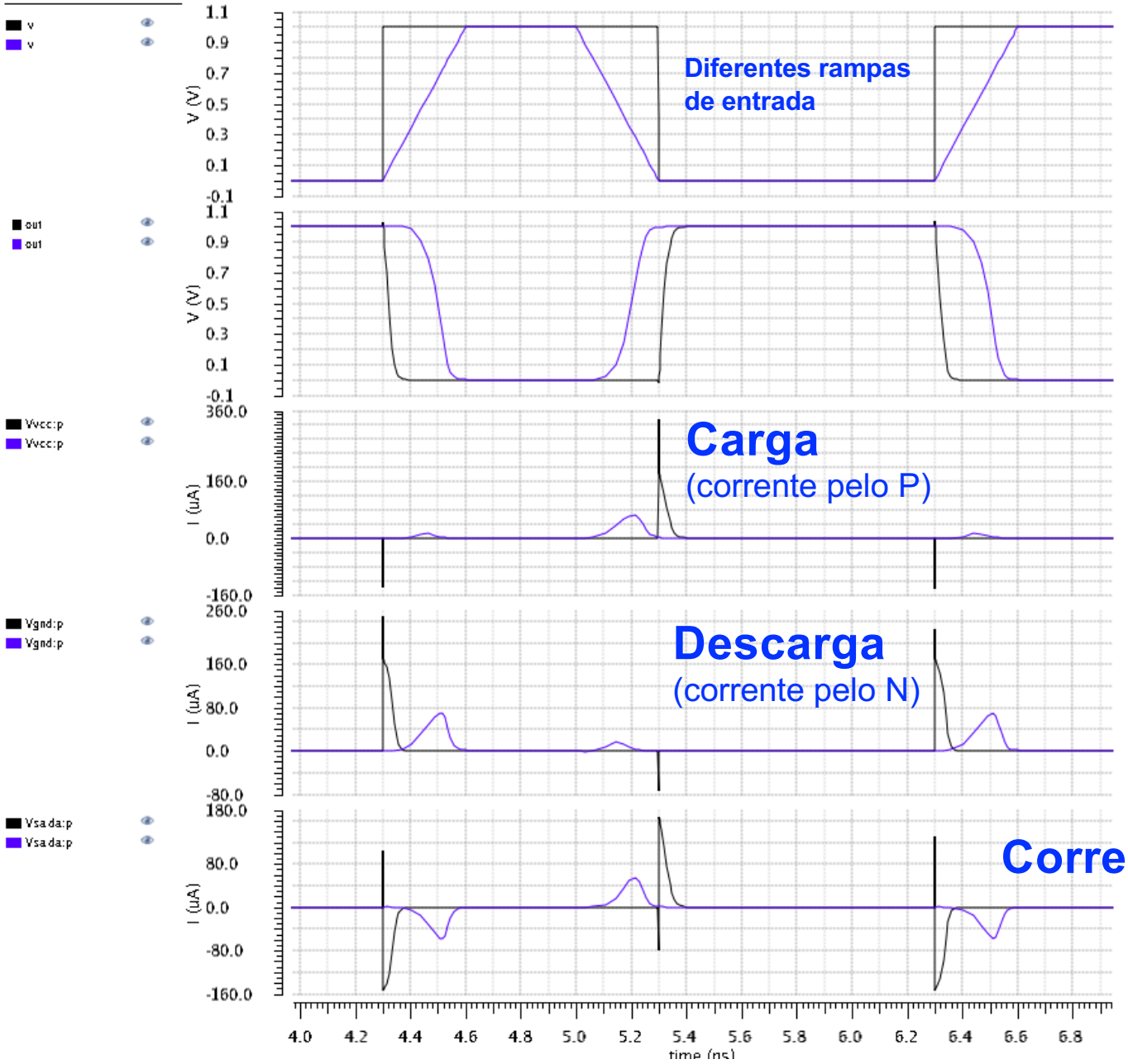
V(in)

V(out)

I(p)

I(n)

I(out)



Diferentes rampas de entrada

Carga
(corrente pelo P)

Descarga
(corrente pelo N)

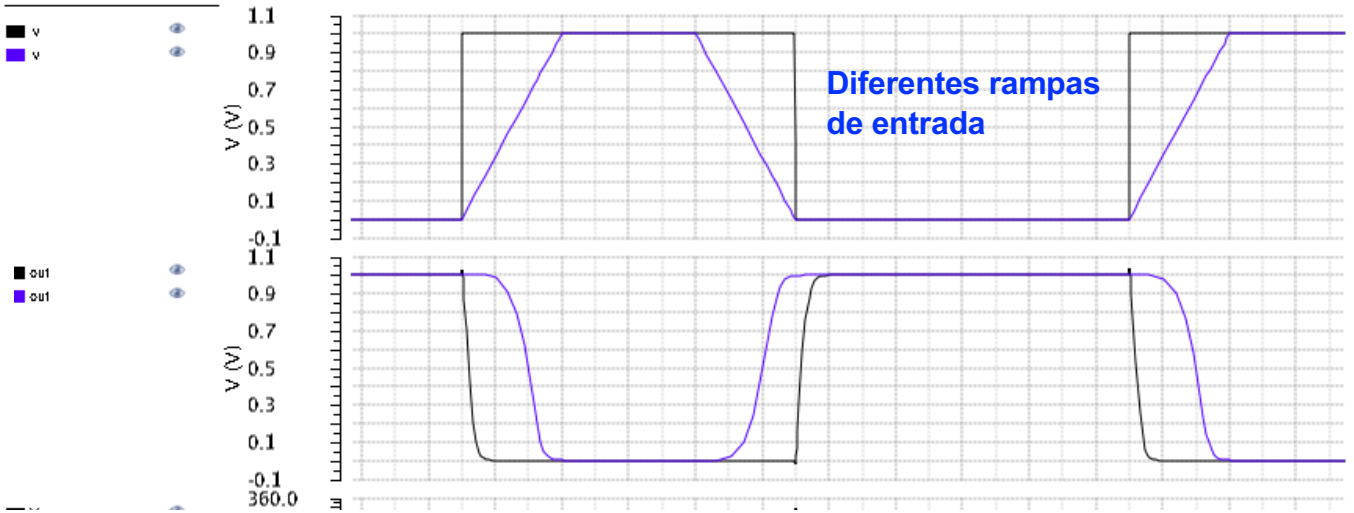
Corrente na saída

Inversor CMOS

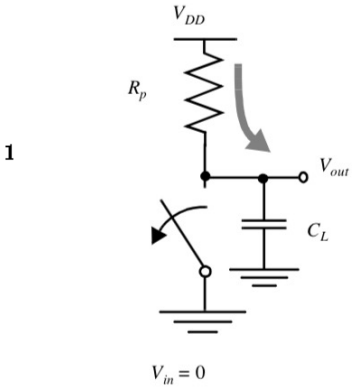
Efeito da rampa

V(in)

V(out)

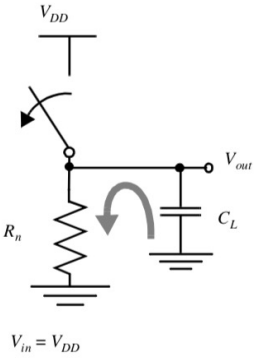


Entrada 0 satura o T_P



(a) Low-to-high

Entrada 1 satura o T_n



(b) High-to-low

Rampa "rápida" (baixo *slew*)

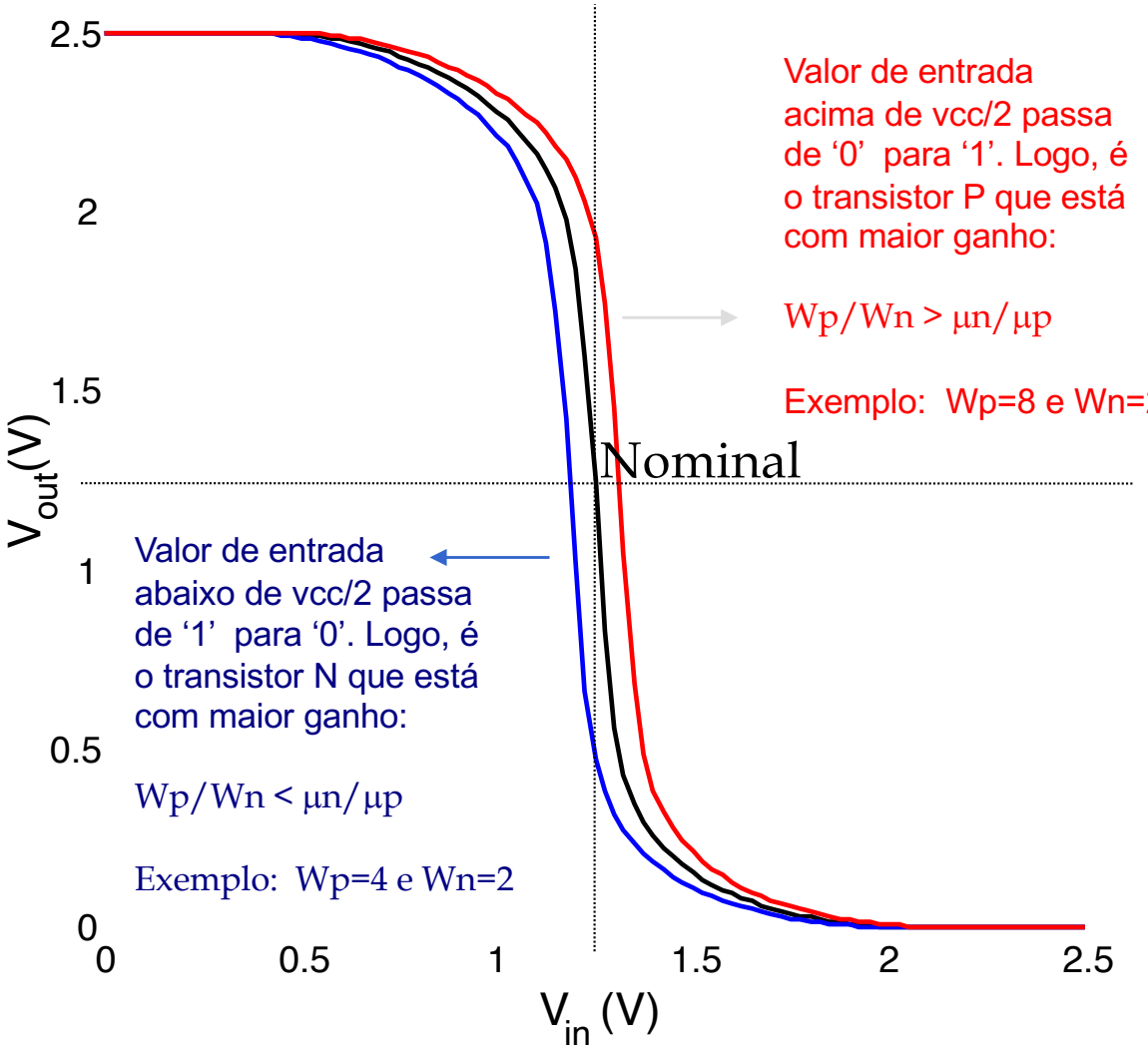
td = 19.689 ps
ts = 18.981 ps
tot_power = 2.82e-06

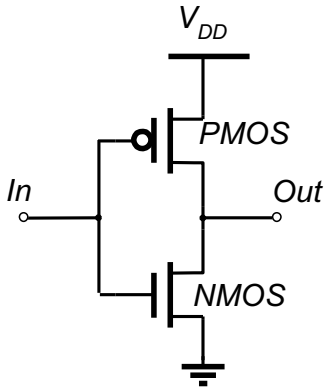
Rampa "lenta" (alto *slew*)

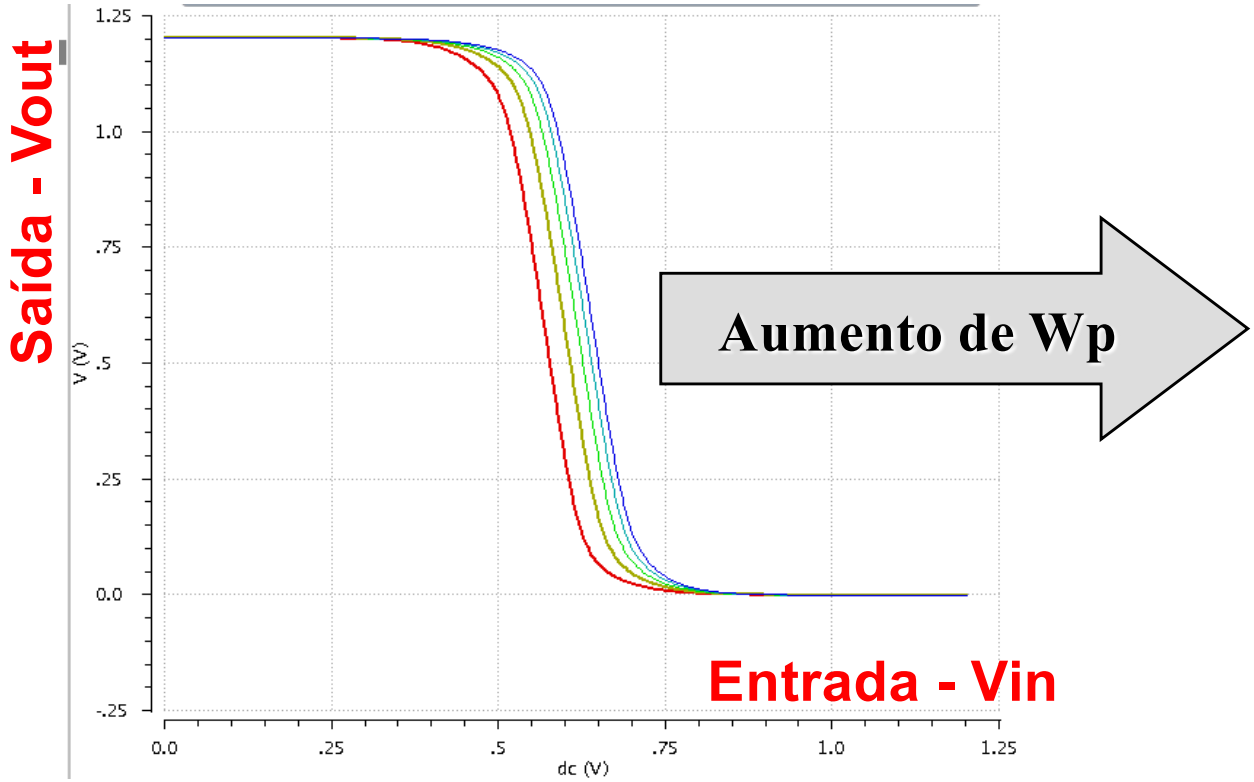
td = 49.1946 ps
ts = 52.0563 ps
tot_power = 3.87e-06 (+37%)

Variação do Tamanho do Transistor - W

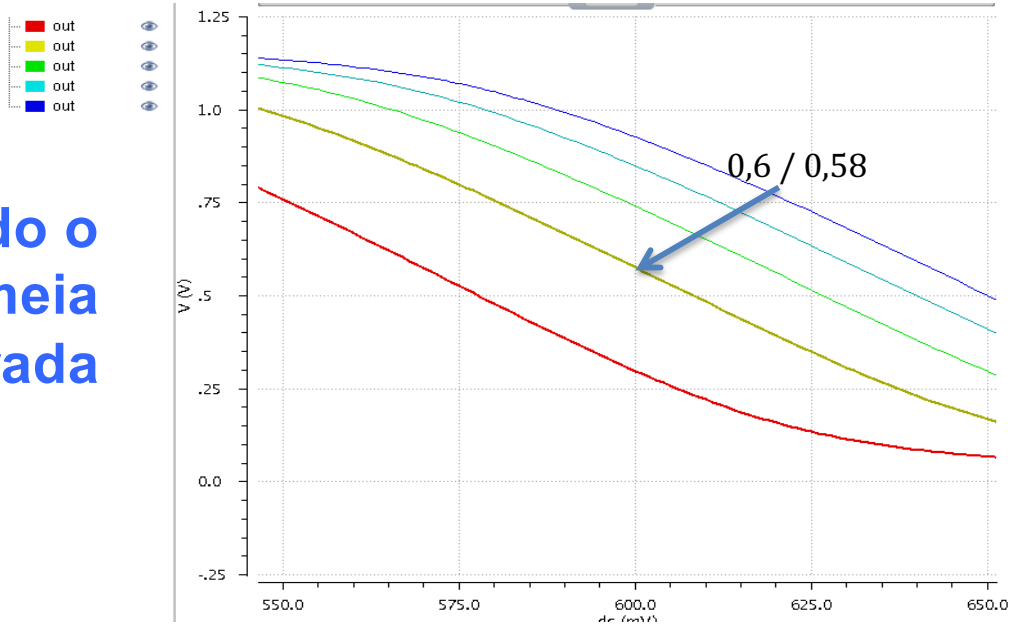
Nominal: relação entre Wp/Wn igual a relação da mobilidade μn/μp. Exemplo:
- Wp= 6, Wn=2 e μn/μp=3





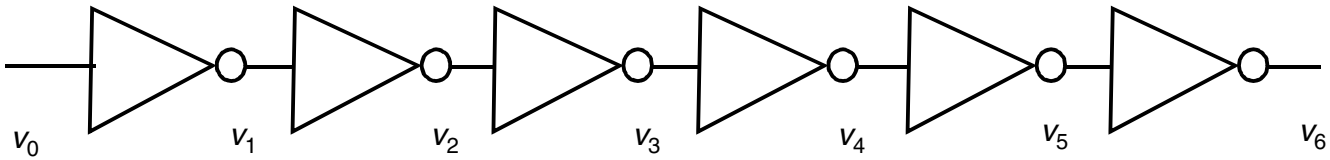


Zoom mostrando o chaveamento na meia excursão do sinal de entrada



Inversor

Propriedade de Regeneração



cadeia de inversores

Inversor pode ser visto como um amplificador

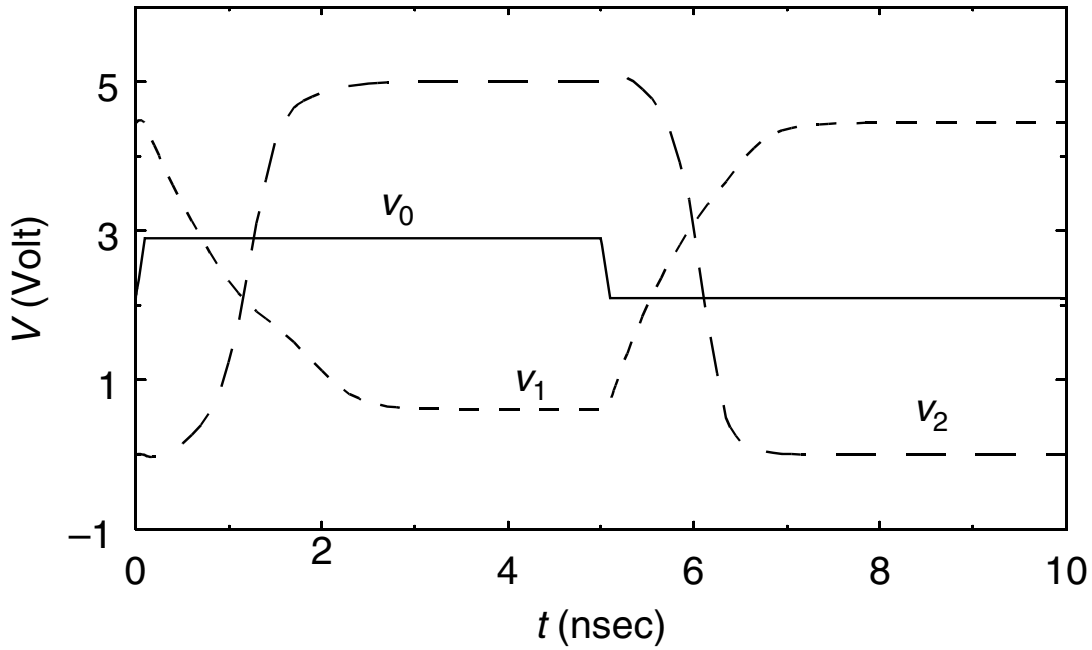
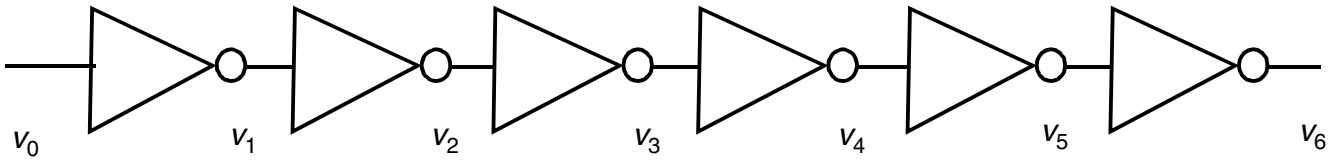


Figure 1.14 The regenerative property.

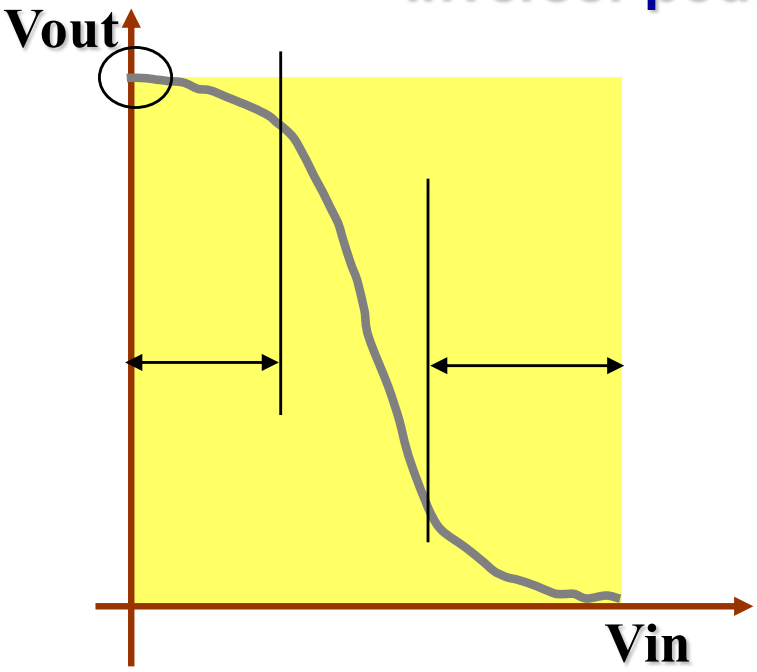
Inversor

Propriedade de Regeneração

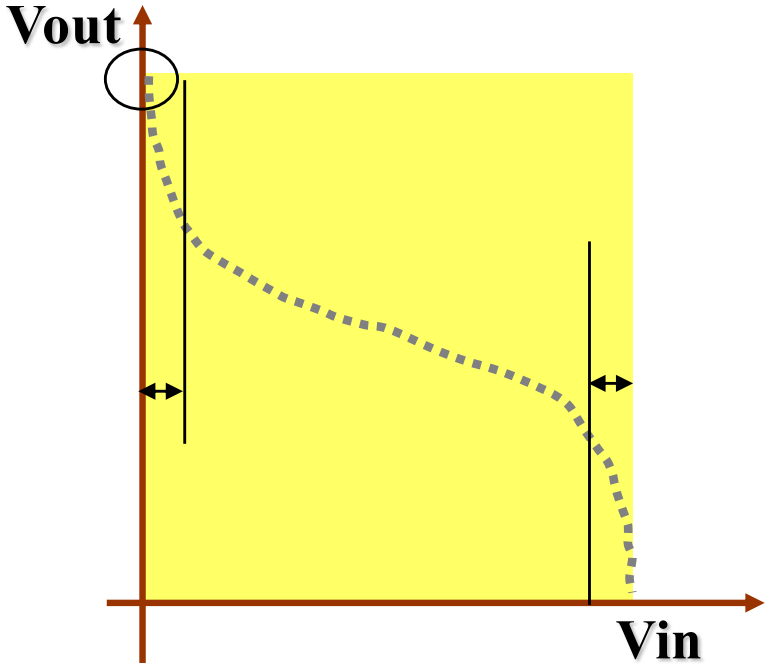


cadeia de inversores

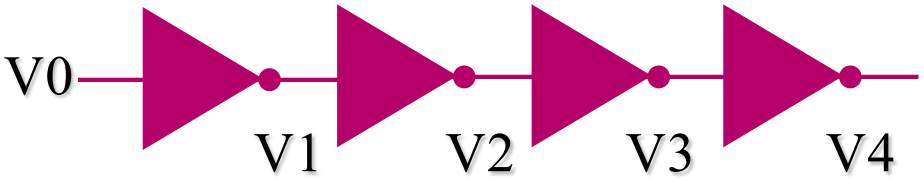
Inversor pode ser visto como um amplificador

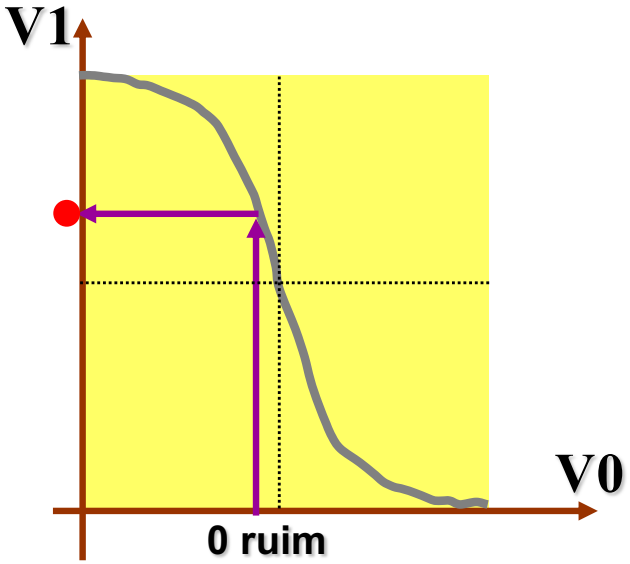


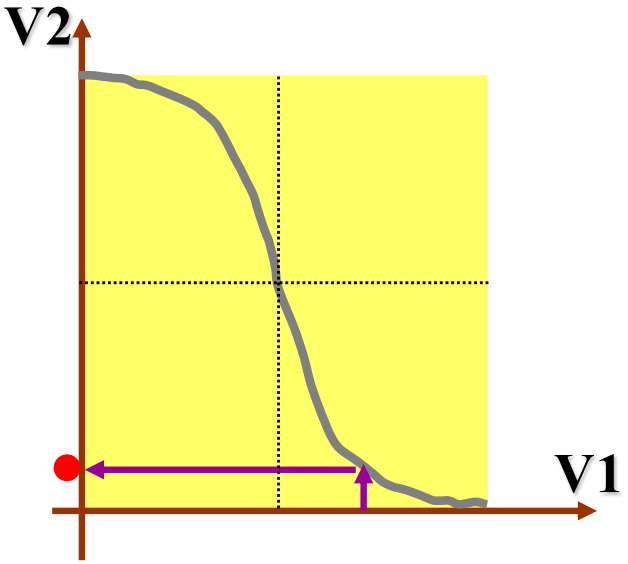
porta com regeneração (alta margem de ruído)

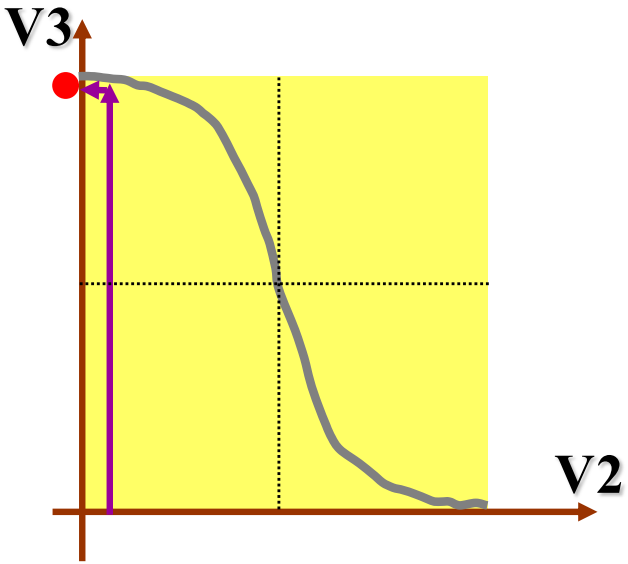


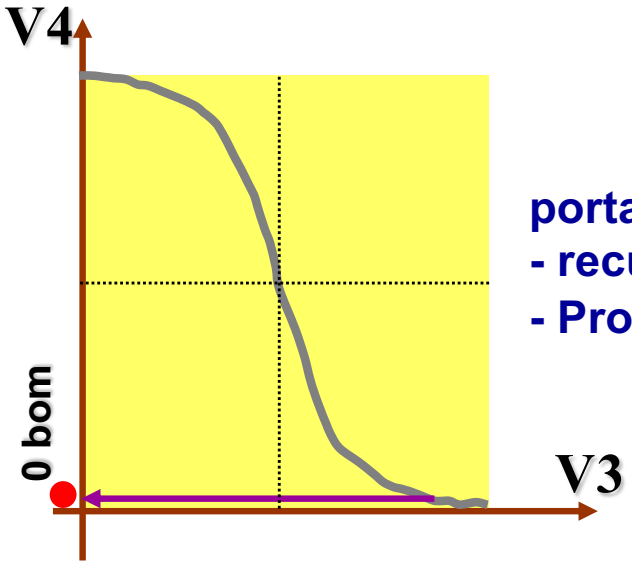
porta sem regeneração (baixa margem de ruído)







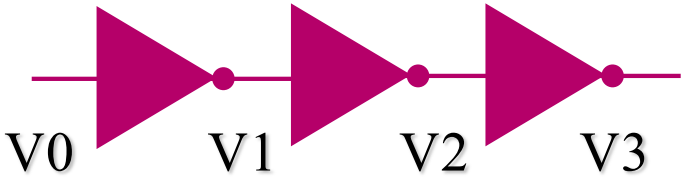




porta com regeneração
- recuperação do nível alto
- Propriedade de amplificação

Inversor

Propriedade de Regeneração



Excursão do sinal de entrada: 0 e 1.2 V

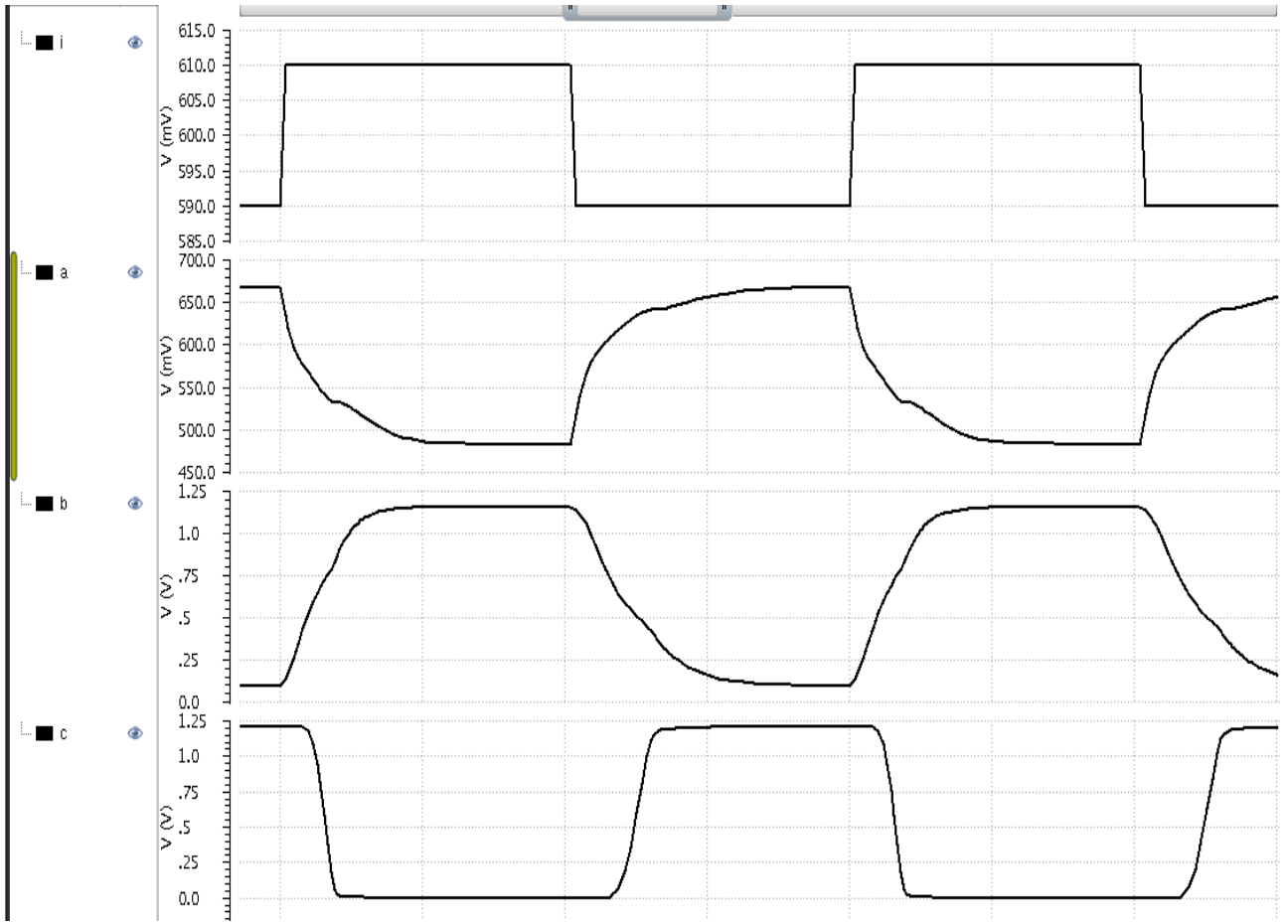
V0 (0.59 – 0.61 V)

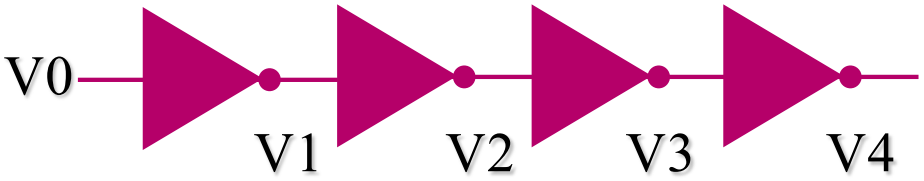
Entrada muito "ruim", próxima à meia excursão do sinal de entrada

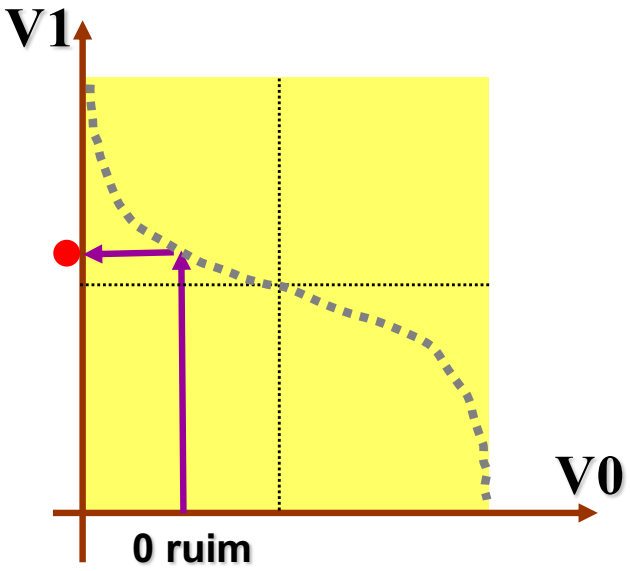
V1 (0.50 – 0.67 V)

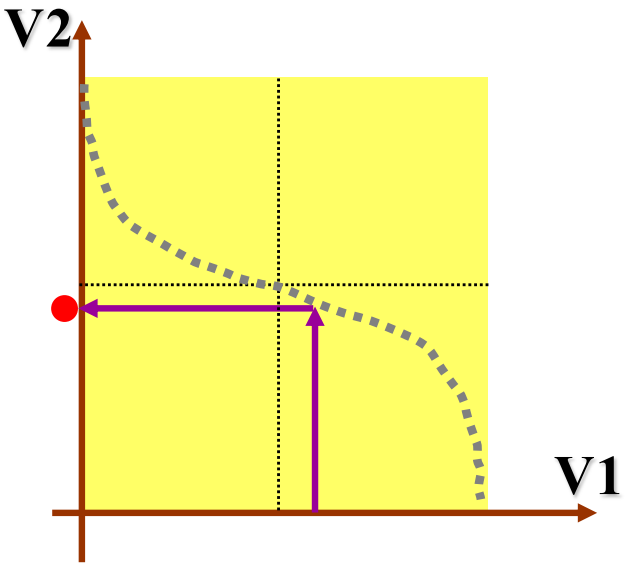
V2 (0.10 – 1.1 V)

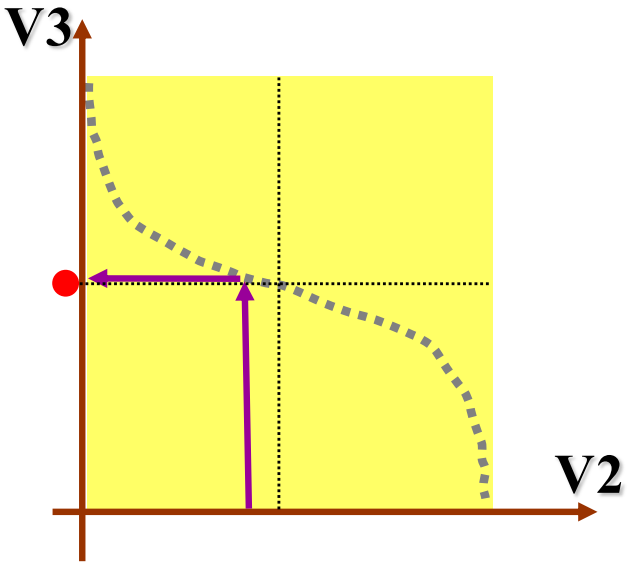
V3 (0 – 1.2 V)

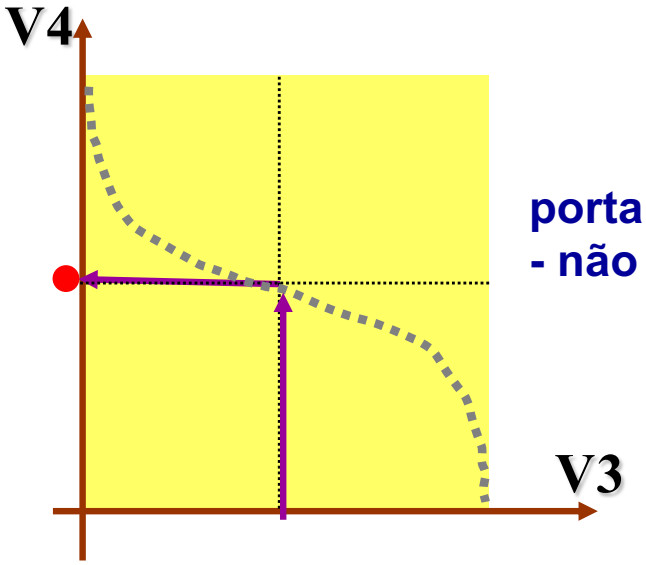








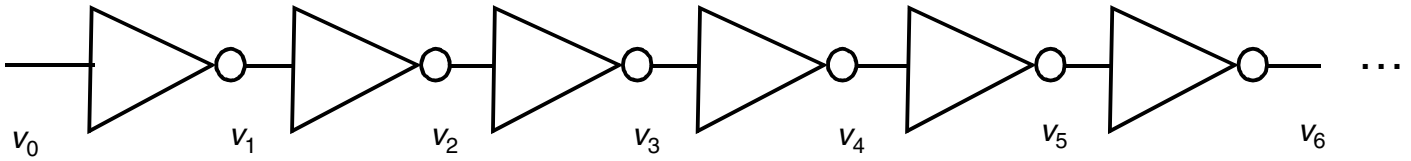


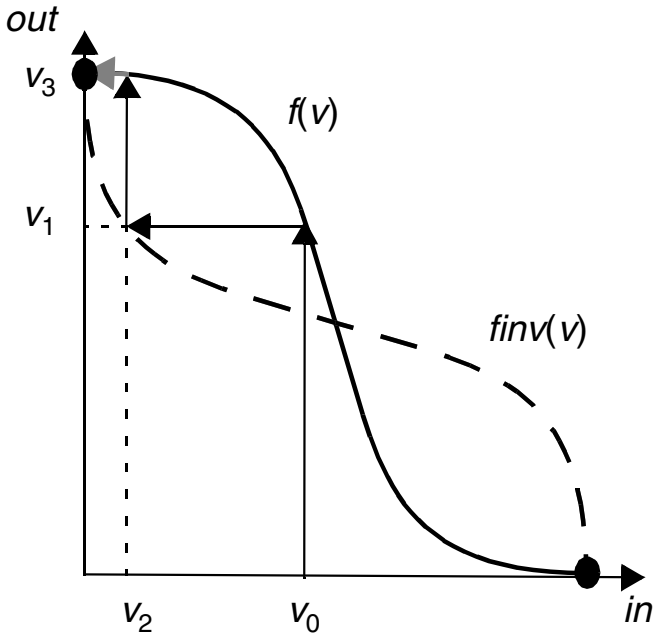


porta sem regeneração
- não recupera o nível alto

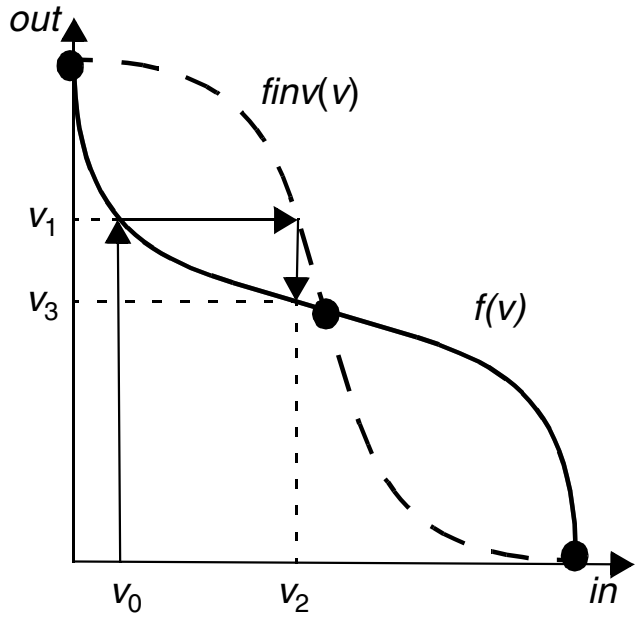
Inversor

Propriedade de Regeneração





(a) Regenerative gate



(b) Nonregenerative gate

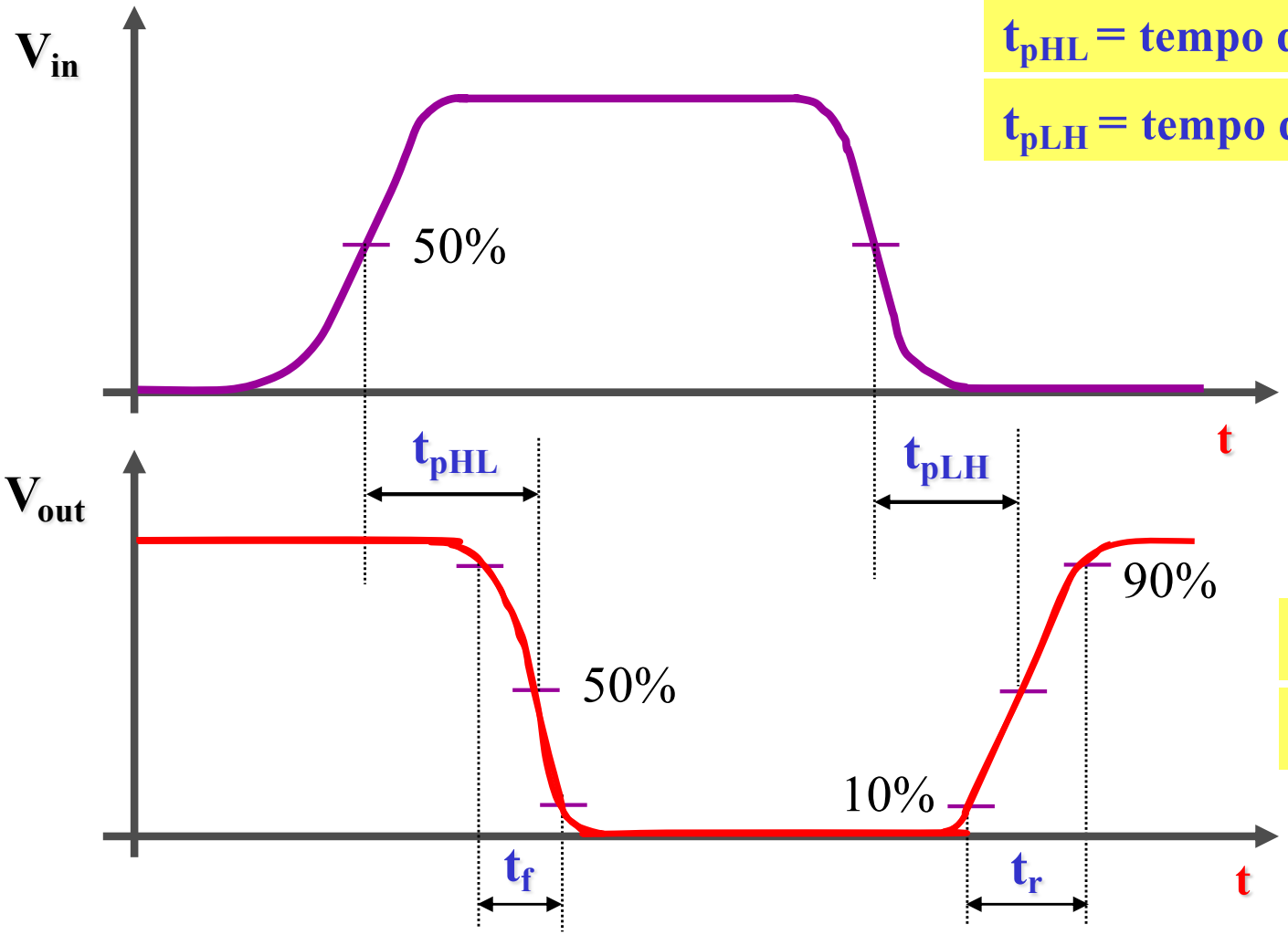
Figure 1.15 Conditions for regeneration.

porta com regeneração (alta margem de ruído)

porta sem regeneração (baixa margem de ruído)

Inversor

Definição de Atrasos



t_{pHL} = tempo de propagação 1 ➡ 0

t_{pLH} = tempo de propagação 0 ➡ 1

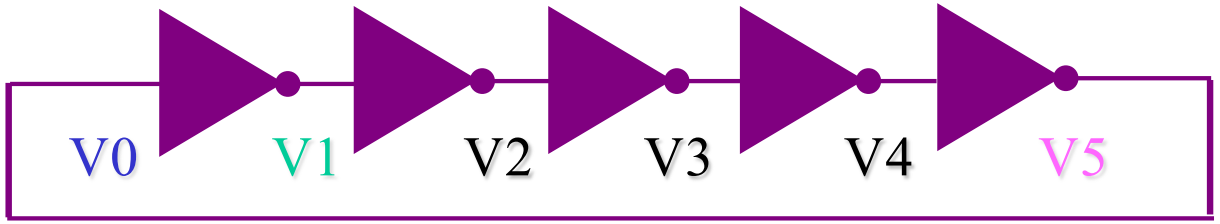
$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

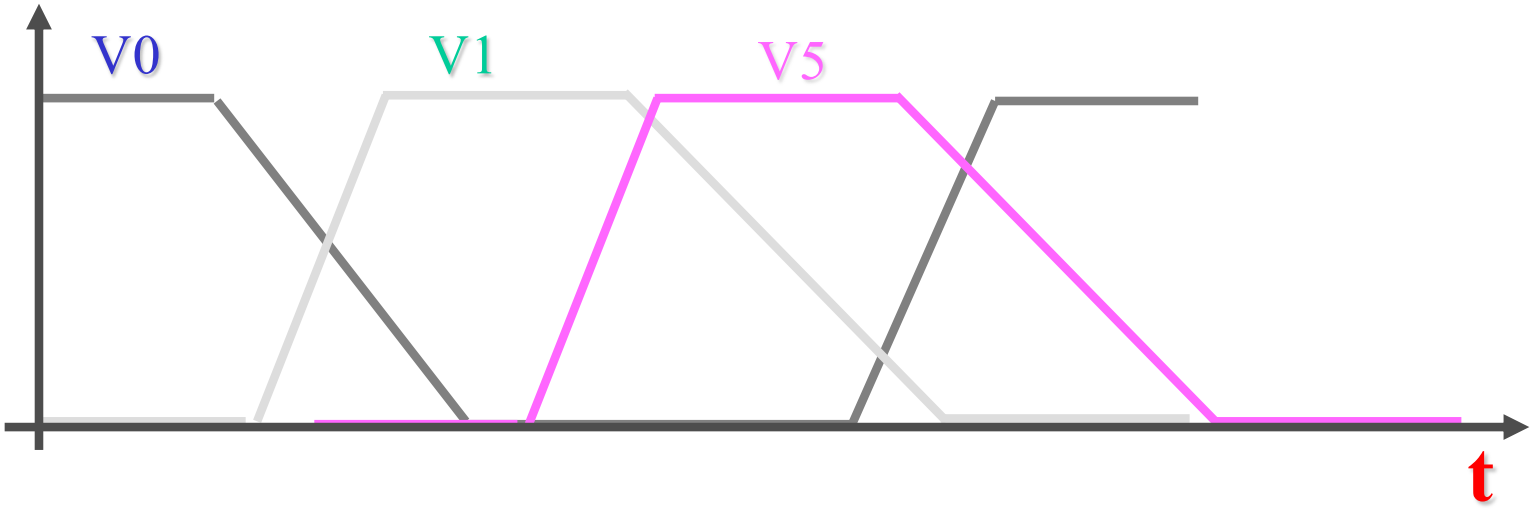
t_f = tempo de descida

t_r = tempo de subida

Inversor

Oscilador em Anel

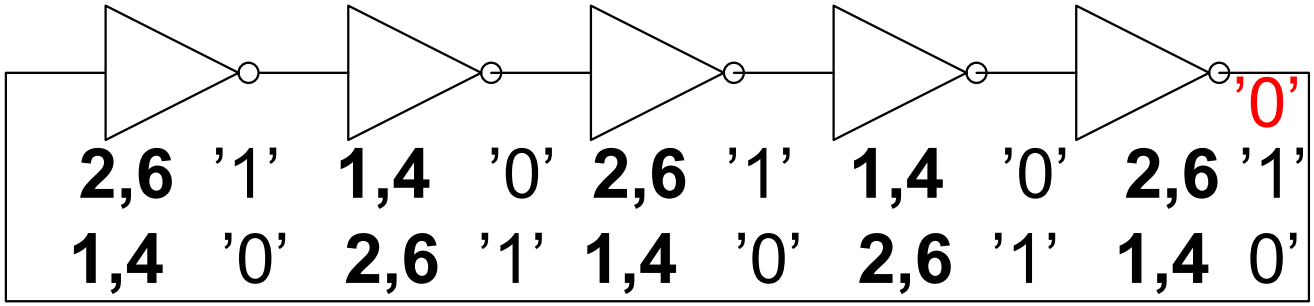




$T = 2 \times t_p \times N$

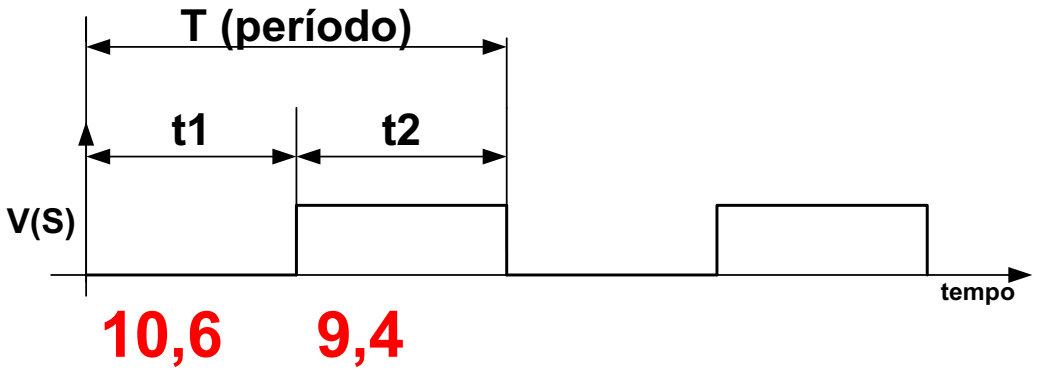
T = período do oscilador

Considere um oscilador em anel de 5 estágios, tendo o inversor tr=2,6 ns (tempo de propagação de subida de um inversor) e tf=1,4 ns (tempo de propagação de descida de um inversor).



Fica em '0' por 10,6 ns

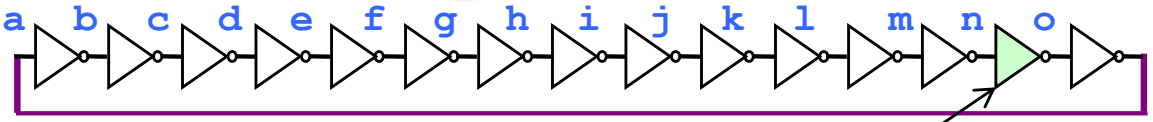
Fica em '1' por 9,4 ns



T = 20 ns

f = 50 MHz

Oscilador com 15 estágios



Tempo de propagação de um inversor

```
.measure tran tf   trig v(n)   val=0.6   td=1n rise = 10
+                  targ v(o)   val=0.6         fall = 10
.measure tran tr   trig v(n)   val=0.6   td=1n fall = 10
+                  targ v(o)   val=0.6         rise = 10
```

RESULTADO:

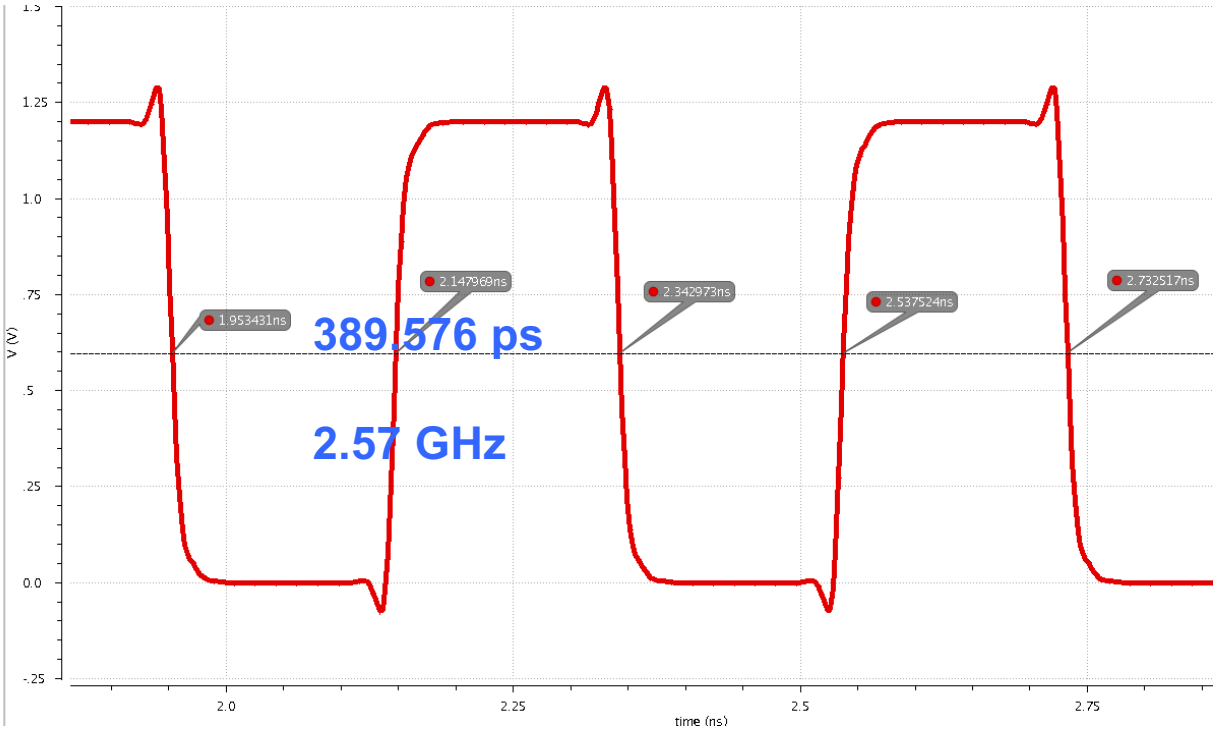
```
tf =  1.31323e-11
tr =  1.29394e-11
```

Tp = 12,986 ps

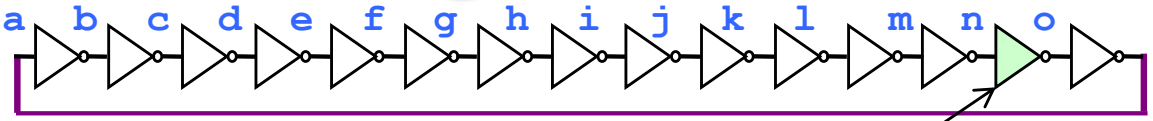
T = 2 * Tp * 15 = 389,576 ps

Dica:

.ic v(a)=1.2



Oscilador com 15 estágios



Tempo de propagação de um inversor

```
.measure tran tf   trig v(n)   val=0.6   td=1n rise = 10
+                  targ v(o)   val=0.6         fall = 10
.measure tran tr   trig v(n)   val=0.6   td=1n fall = 10
+                  targ v(o)   val=0.6         rise = 10
```

```
.measure tran periodo   param = '(tf+tr) * 1e9 * 15'
.measure tran freq      param = '1/periodo'
```

Medindo diretamente o período:

```
.measure tran periodo_o   trig v(o)   val=0.6   td=1n rise = 2
+                         targ v(o)   val=0.6         rise = 3
```

Resultado do *measure*

freq = 2.56689 ➔ frequência de oscilação igual a 2,57 GHz
periodo = 0.389576
periodo_o = 3.89551 e-10

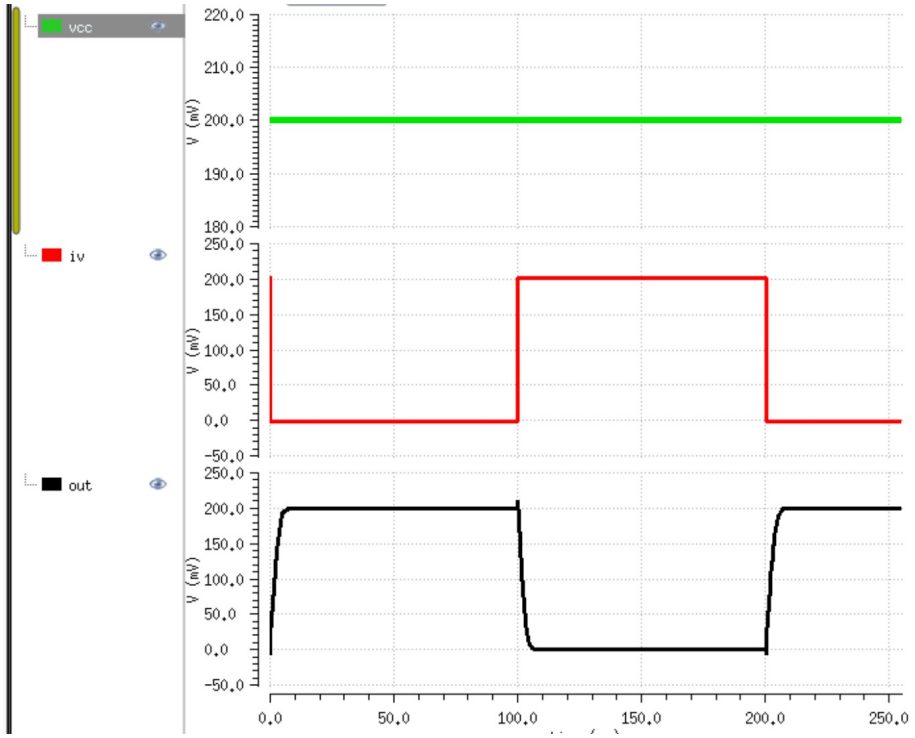
Sub-threshold

Vcc=1.0 → tp ≈12 ps

Vcc=0.2 → tp ≈1.8 ns = 1800 ps

Funciona corretamente, mas

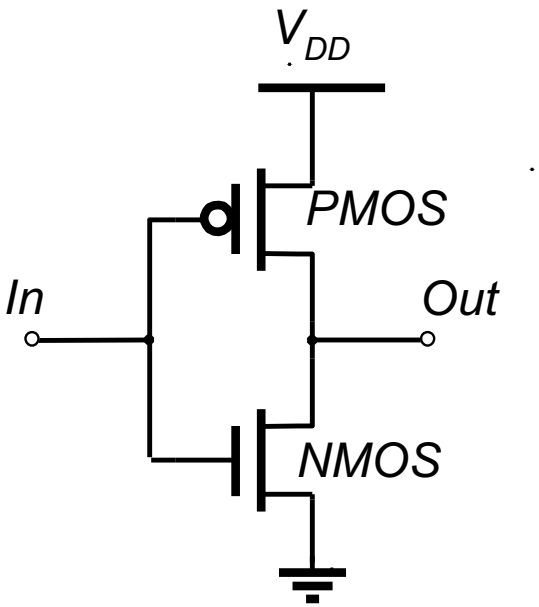
- 150x mais lento
- baixíssima margem de ruído

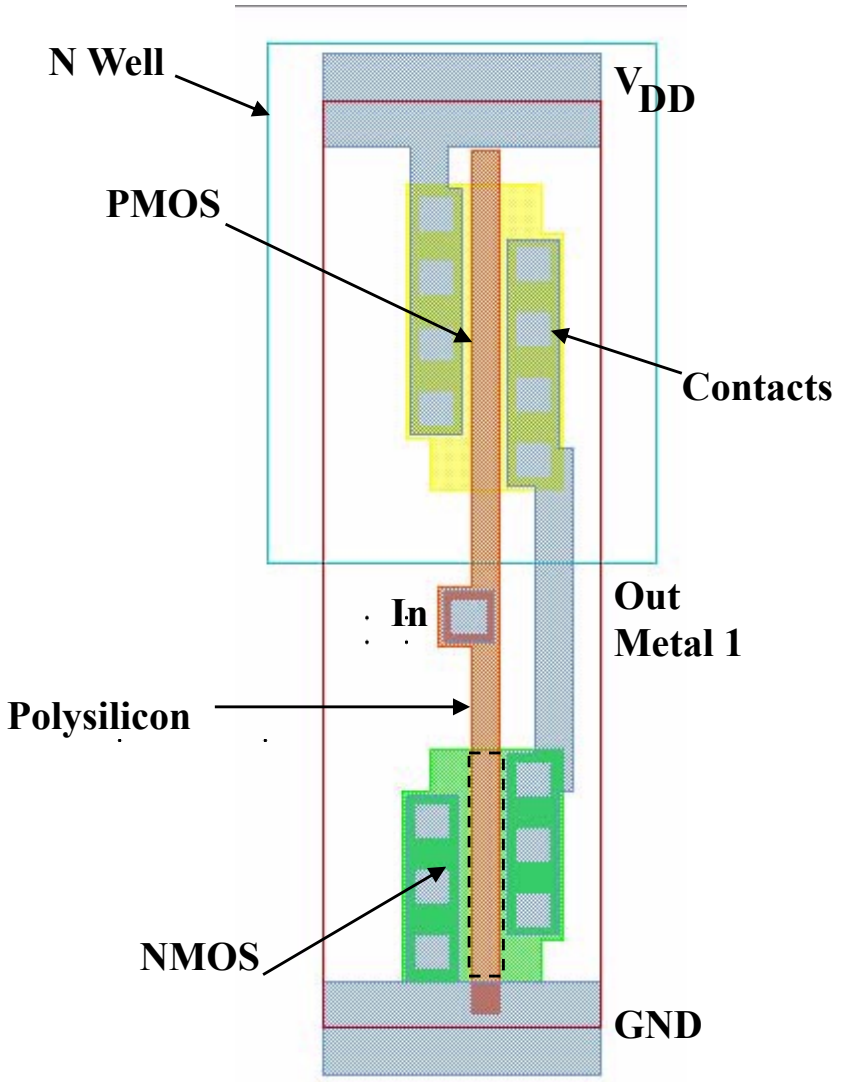



```
M1 vcc iv out   vcc   psvtgp w=wp l=0.06
M2 0   iv out   0     nsvtgp w=wn l=0.06

vcc vcc  0  dc 0.2
vin1 iv  0  pulse (0.2 0 0 0.05N 0.05N 100n 200n)

C1  out  0 4fF
```

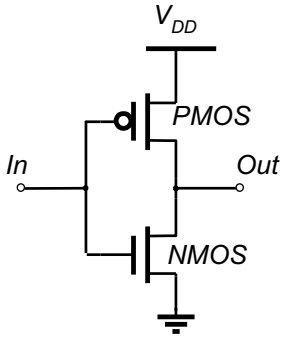
```
Measurement Name   :  transient1
Analysis Type      :  tran
diff           = -154.777
phl            = 1.71937e-09
plh            = 1.87415e-09
```

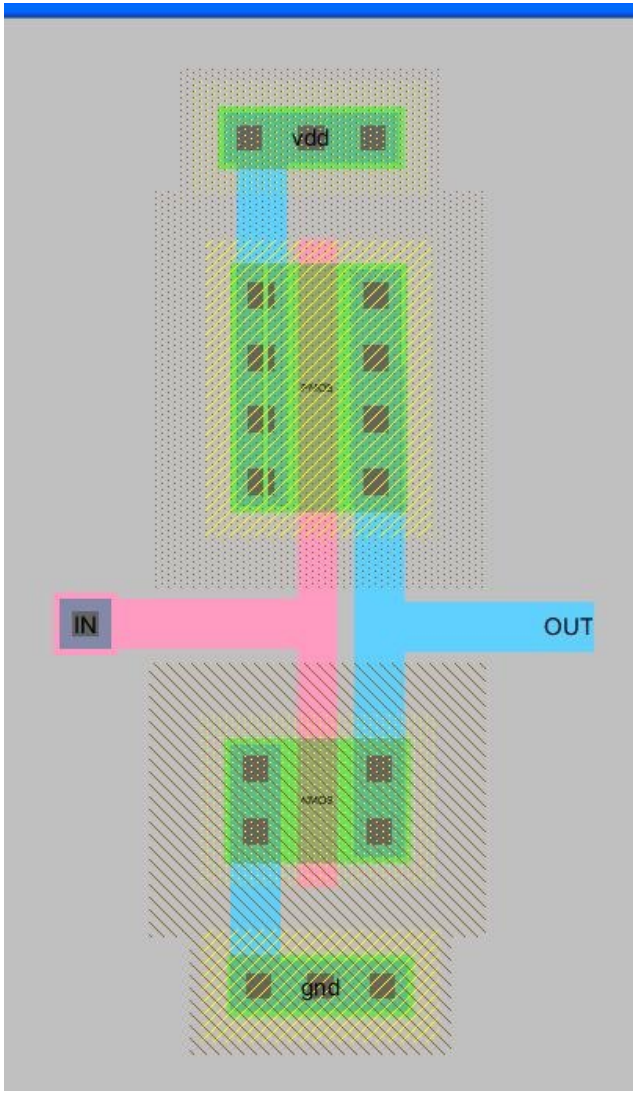
CMOS Inverter

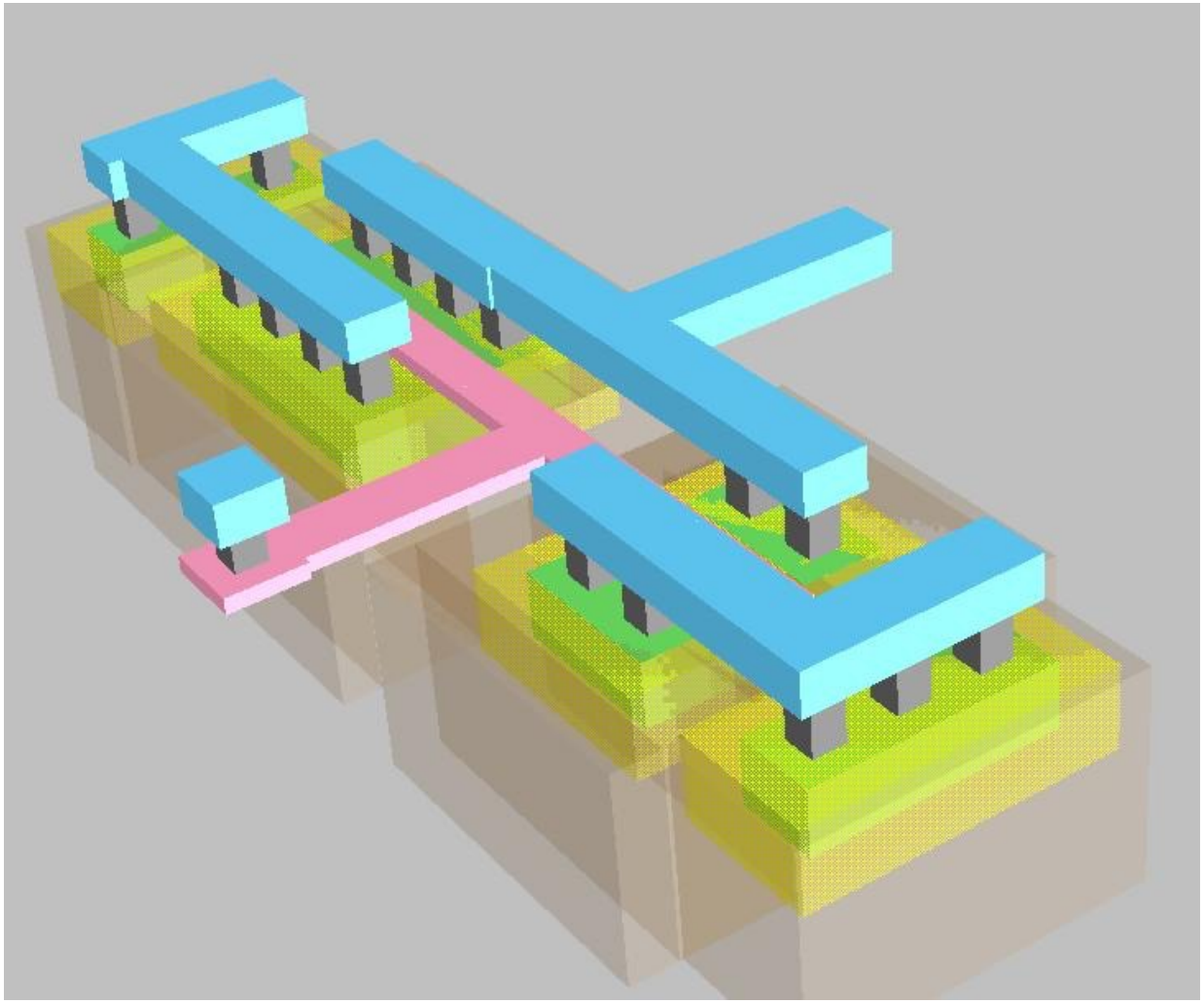




CMOS Inverter







http://cmosedu.com/jbaker/courses/ee421L/f13/students/lamorea3/Lab5/lab5.html

CMOS Inverter

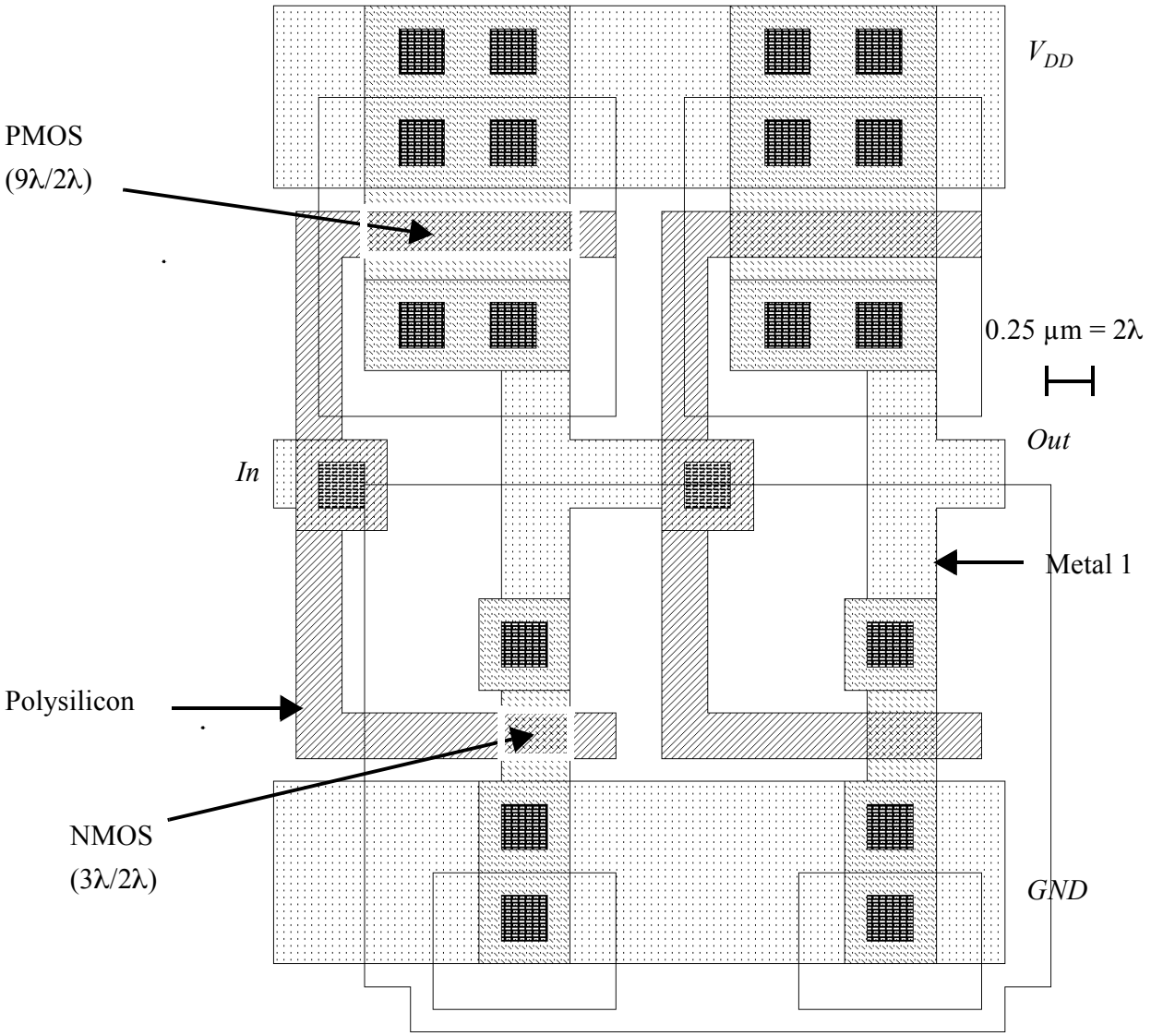
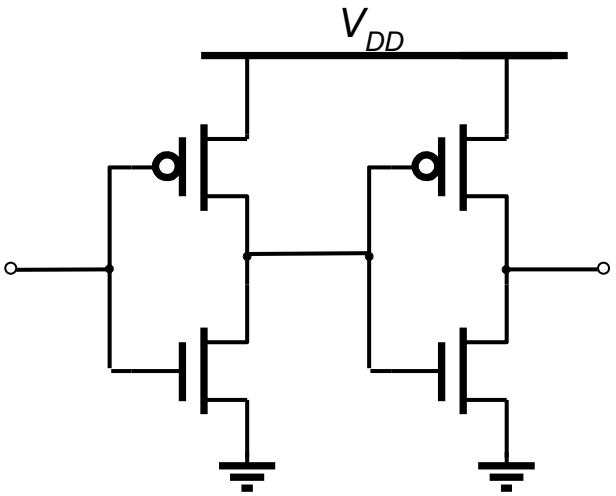
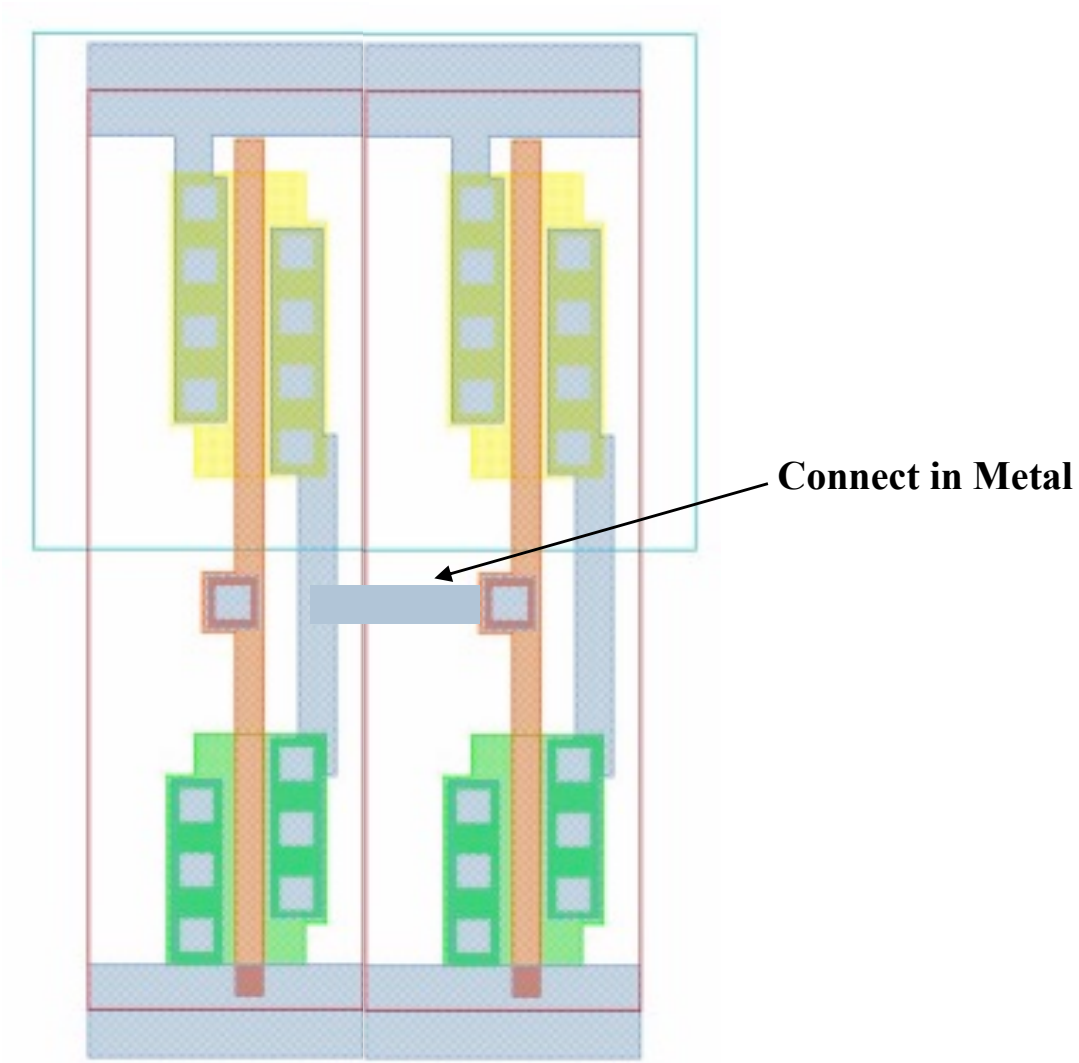


Figure 5.15 Layout of two chained, minimum-size inverters using SCMOS Design Rules (see also Color-plate 6).

Two Inverters

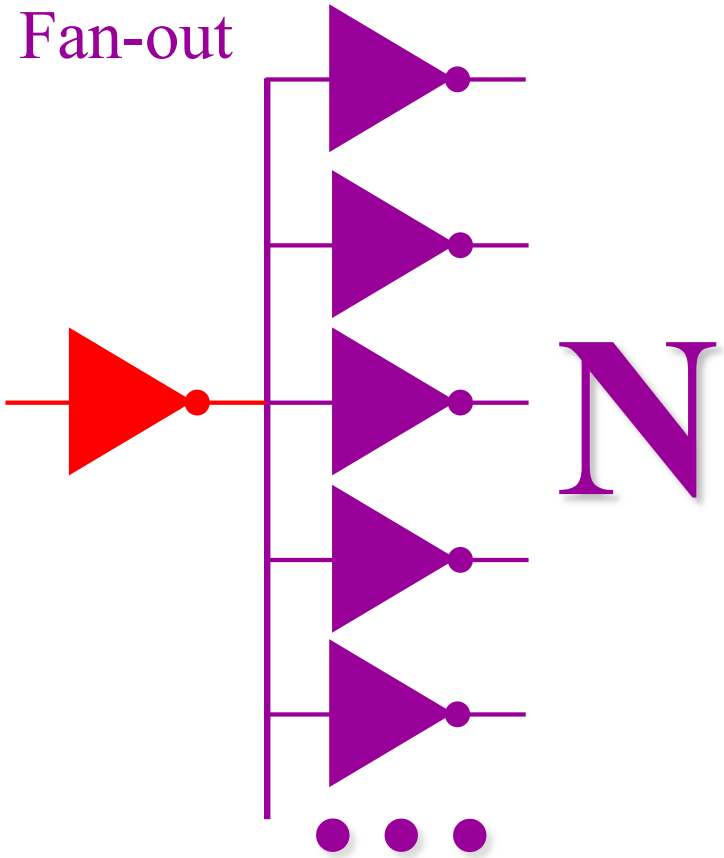
- Share power and ground
- Abut cells



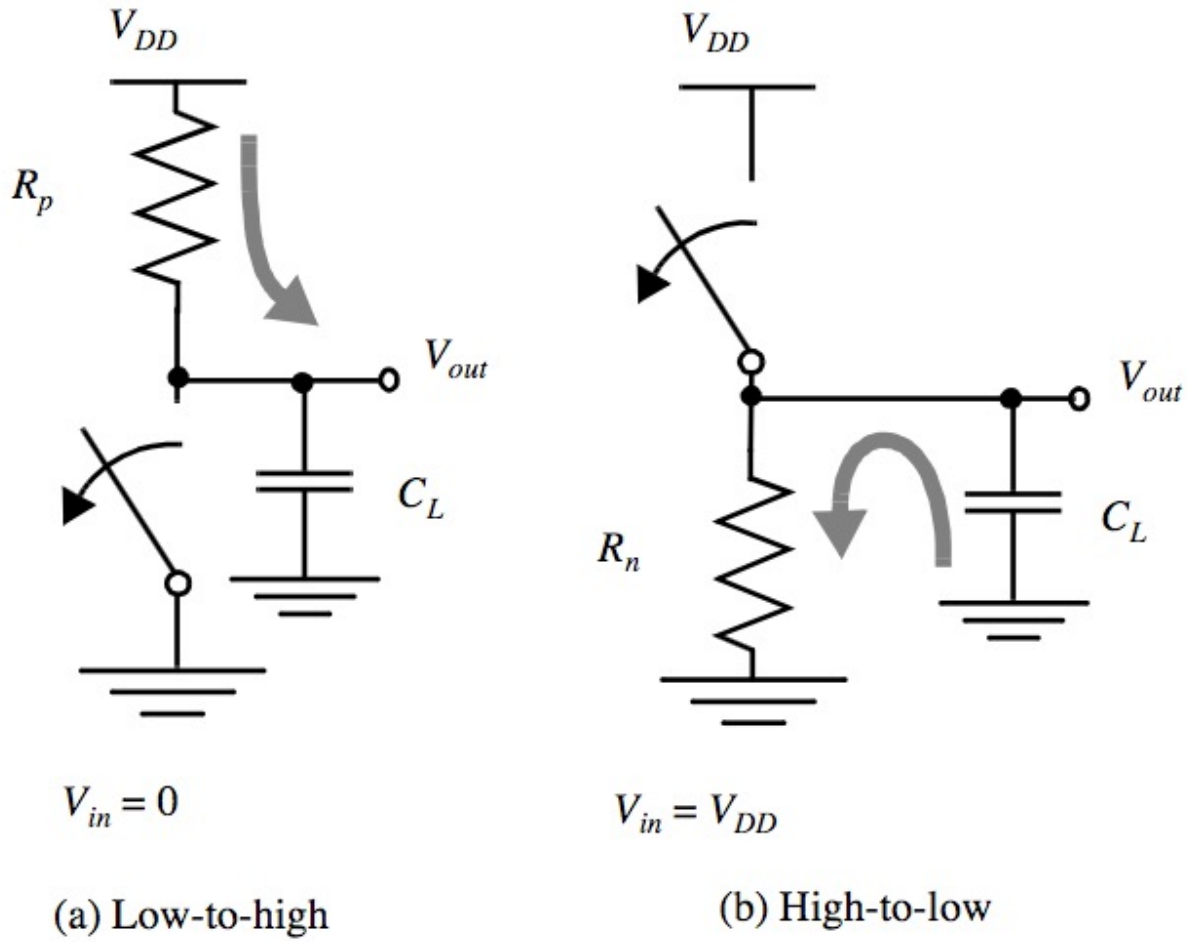


Inversor

Fan-in e Fan-out



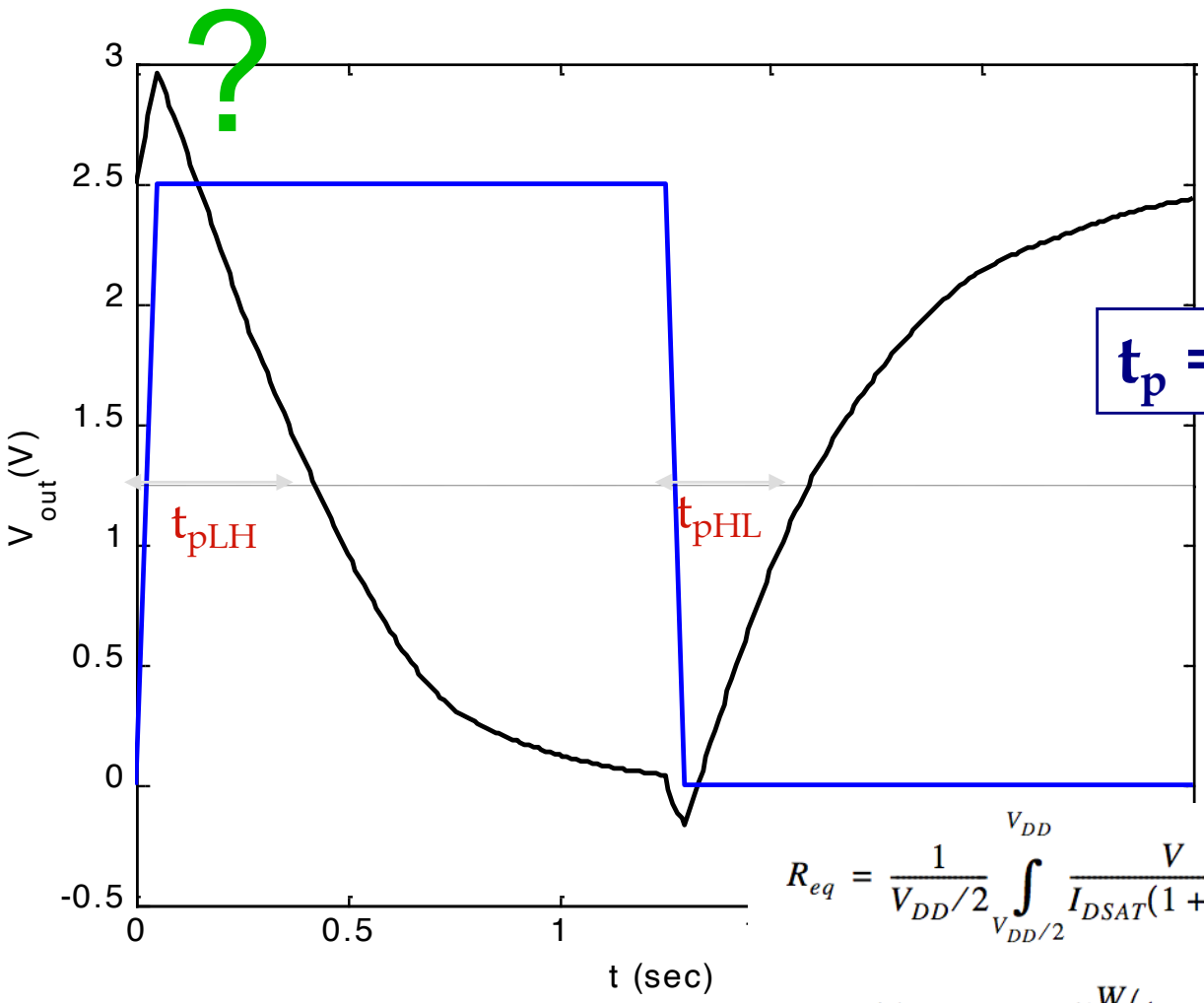
CMOS Inverter Propagation Delay



$$t_{pHL} = f(R_{on}.C_L)$$
$$= 0.69\ R_{on}C_L$$

Figure 5.6 Switch model of dynamic behavior of static CMOS inverter.

Transient Response



$$t_p = 0.69\, C_L\, (R_{eqn}+R_{eqp})/2$$

$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right) \qquad (5.17)$$

with $I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$

Inversor

Dissipação de Potência

- **Potência de pico**: importante para dimensionar as linhas de alimentação

$$P_{peak} = i_{peak} V_{supply}$$

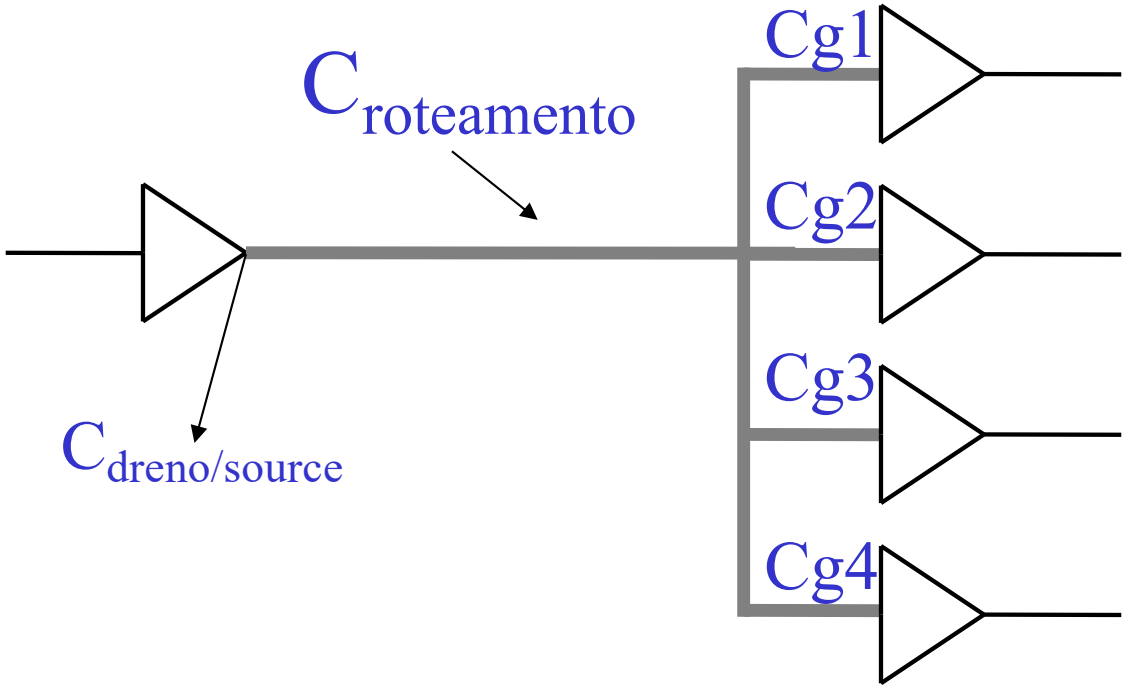
- **Potência média**: importante para cálculo de dissipação de calor e de dimensionamento das baterias

$$P_{av} = \frac{1}{T}\int_0^T p(t)dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)dt$$

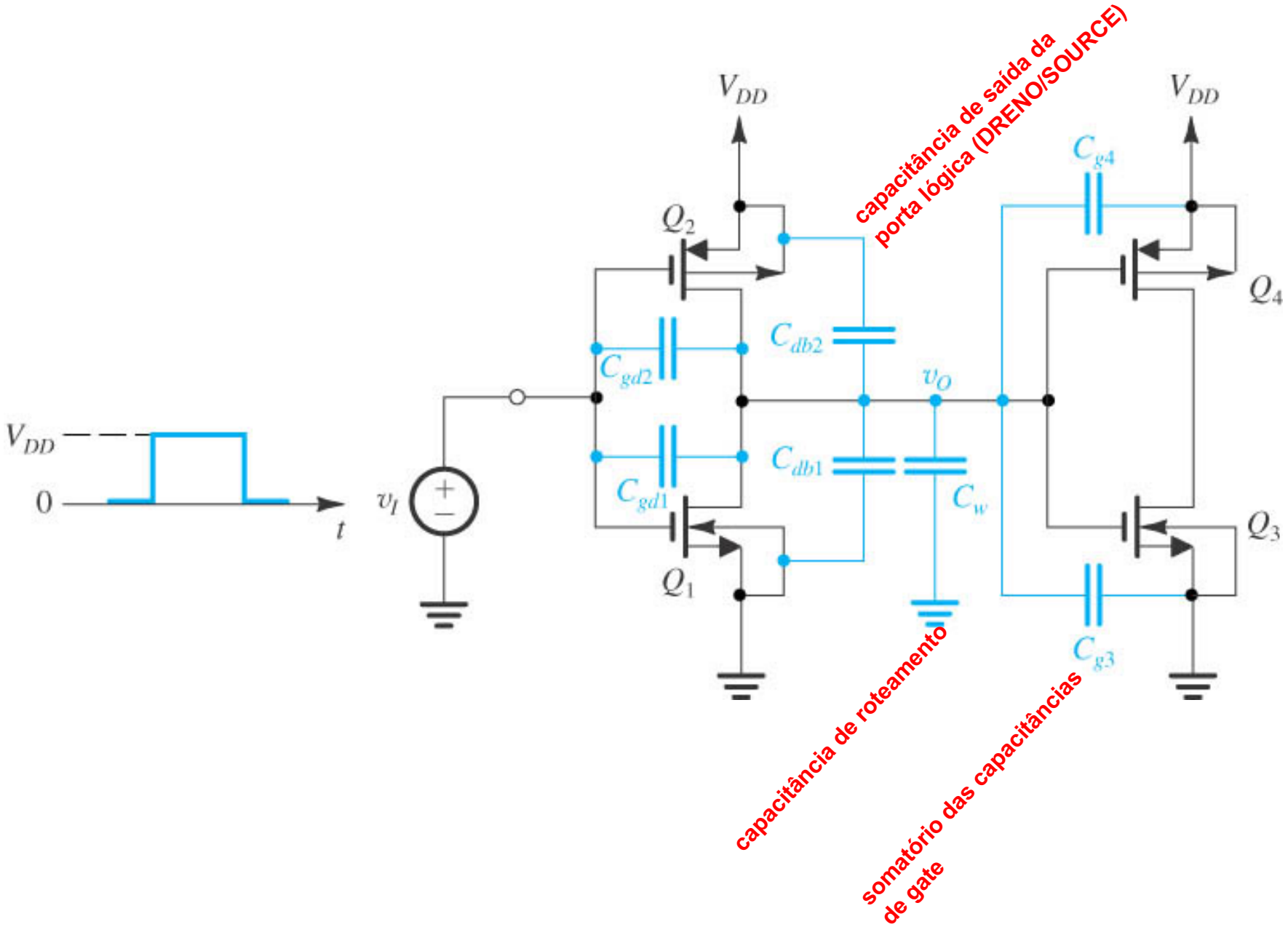
  - **Componentes da correnete:**
    - Estático: devido às correntes de fuga
    - Dinâmico: proporcional ao chaveamento do inversor

CAPACITÂNCIAS

- A capacitância de um sinal é composta por:
  - capacitância de saída da porta lógica (DRENO/SOURCE)
  - capacitância de roteamento
  - somatório das capacitâncias de gate conectadas ao sinal



Capacitâncias parasitas



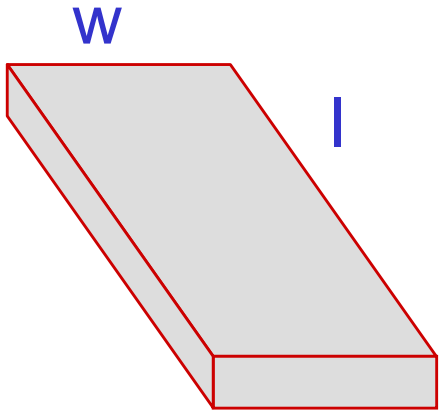
Roteamento

- A carga do roteamento deve ser acrescida ao C_L na equação do atraso das portas.
- Hoje o atraso devido ao roteamento é da mesma ordem de grandeza do atraso das portas lógicas.

$r \rightarrow \Omega / \mu m$ (resistência por unidade de comprimento)

$c \rightarrow F / \mu m$ (capacitância por unidade de comprimento)

$$atraso\ no\ fio : t = 0.7.\frac{r.c.l^2}{2}$$



Roteamento

- linhas longas
  - Supondo: r=20Ω/μm e c=0,4 fF/ μ m
  - Atraso em uma linha de 1000 μ m

    $t = 0.35 \cdot 20 \cdot 0{,}4e\text{-}15 \cdot (1000)^2 = 2.8ns$
  - Atraso em uma linha de 2000 μ m

    $t = 0.35 \cdot 20 \cdot 0{,}4e\text{-}15 \cdot (2000)^2 = 11.2ns$

  - **Solução indicada para acelerar a linha de 2000 μm:**