PONTIFÍCIA UNIVERSIDADE CATÓLICA DO RIO GRANDE DO SUL
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AN ANALYSIS OF THE FABRICATION, CHARACTERIZATION AND APPLICATION OF ACADEMICALLY DEVELOPED SOLAR CELLS

MARCELO MELO LINCK

END OF TERM WORK

ADVISOR: PROF. DR. FERNANDO GEHM MORAES

PORTO ALEGRE
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End of Term work presented as part of the activities to obtain a degree of Computer Engineering at the Faculty of Engineering in the Pontifical Catholic University of Rio Grande do Sul.

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ABSTRACT

Most all of the electrical energy produced today comes from the burning of fossil fuels, which are a limited energy resource and calculations predict its ending not too long from now. A strong alternative for the generation of energy is the solar cell, a device capable of converting solar energy – from the sun, an infinite energy source – into electrical power using the photovoltaic effect. Most commonly, solar cells are classified according to its efficiency, a ratio between the output power and the power of the input light. Lately, efficiencies up to 25.6% for silicon solar cell at 1-sun [TOM14] and 44.4% for a multi-junction III-V [SAS13] at concentrated sunlight were achieved. This work presents an overview on the most common solar cell fabrication processes, and details one separate sequence that was performed by the author to fabricate four solar devices. These devices are then electrically characterized and compared to an existing solar cell fabricated through an industrial process at the PUC-RS campus. This characterization and comparison classifies the solar cells performance through the existing devices already available, and defines the limits of the cells for a possible application.

"The true sign of intelligence
is not knowledge
but imagination."
Albert Einstein

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List of Symbols and Abbreviations

$\rho_{\blacksquare}$	Sheet Resistivity
a-Si	Amorphous Silicon
ABES	Brazil Association of Solar Energy
AIST	Japanese National Institute of Advanced Industrial Science and Technology
AM	Air Mass
ARC	Anti-Reflective Coating
BOE	Buffered Oxide Etch
BSF	Back Surface Field
c-Si	Crystalline Silicon
CB-Solar	Brazilian Center for Development of Solar PV Energy
CVD	Chemical Vapor Deposition
cz-Si	Czochralski Silicon
DI	Deionized
EBE	Electron-Beam Evaporation
EHP	Electron-hole pair
EOT	End of Term
EVA	Ethyl Vinyl Acetate
FACIN	School of Informatics of PUC-RS
FENG	School of Engineering of PUC-RS
FF	Fill Factor
FhG-ISE	Fraunhofer-Institut für Solare Energiesysteme
fz-Si	Float Zone Silicon
HWCVD	Hot-Wire Chemical Vapor Deposition
I	Net Current
i-Si	Intrinsic Silicon
I_0	Dark Current
IBC	Interdigitated Back Contact
III-V	Elements from column III to V on the periodic table
I_L	Light Generated Current
I_M	Maximum Power Current
I_{SC}	Short-Circuit Current
k	Boltzmann Constant
mc-Si	Multi-Crystalline Silicon
MOCVD	Metalorganic Chemical Vapor Deposition
mono-Si	Mono-Crystalline Silicon
M_{PP}	Maximum Power-Point
MSU	Montana State University
n	Ideality Factor
NREL	National Renewable Energy Laboratory
PAE	Phosphoric Acid Etch

pc-Si	Poly-Crystalline Silicon
PECVD	Plasma Enhanced Chemical Vapor Deposition
PERC	Passivated Emitter and rear Contacts
PERL	Passivated Emitter and Rear Locally Diffused
PERT	Passivated Emitter and Rear Totally Diffused
PESC	Passivated Emitter Solar Cell
P_{in}	Input Power from the Sun
PSG	Phosphorous Silicate Glass
PV	Photovoltaic
PVD	Physical Vapor Deposition
q	Charge of a Carrier
RCA	Radio Corporation of America
R_{CH}	Characteristic Resistance
RF	Radio Frequency
R_S	Series Resistance
R_{SH}	Shunt Resistance
SC	Standard Clean
Si	Silicon
T	Temperature in Kelvins
TCO	Transparent Conductive Oxide
TMAH	Tetramethylammonium hydroxide
UNSW	University of New South Wales
UV	Ultra-Violet
V	Voltage/Volts
V_M	Maximum Power Voltage
V_{OC}	Open-Circuit Voltage
η	Efficiency
µc-Si	Micro-Crystalline Silicon
Ω/■	Ohms per square

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1 INTRODUCTION

Solar Energy is, directly or not, the most important energy on Earth. Most animals, as well as plants, need it in order to keep good health and a good life quality, but this energy is not just linked directly to beings' health, but also, as its main power source. For example, fossil fuels are organic material that have stored the sun's energy for a long time, or either the sunlight that heats the air, creating air currents, or wind, which Aeolian Centers use in order to generate electrical energy from mechanical energy. Even the hydropower, which generates electricity by the movement of water, uses the help of evaporation (caused by the sun) [PVC14].

The use of sunlight as a way to generate energy has been receiving attention since the 19th century. It was in 1839 that Becquerel discovered the photovoltaic (PV) effect, which was enforced by Day and Adams in 1887 [CRU05]. However, it was just in the 1950s that the first photovoltaic cell was created, in Bell Laboratories. Through this achievement, the first satellite using solar cells was launched in 1958, called Vanguard I [LOR94]. Unfortunately, due to the low price of fossil fuels, especially the oil, and the elevated cost to produce a single watt using solar energy, solar cells were taken a little aside for a while [SEI83].

Later, during the late 1970s, the solar energy has been taken more seriously again due to the energy crisis and the elevated price of oil. Along this period, the National Photovoltaic Program was initiated in the U.S. and researchers started receiving more funding to the subject [SEI83]. Since then, the goal of the photovoltaic area is to gradually increase cell's efficiency, and develop low cost and efficient ways to fabricate good quality devices.

Meanwhile, the history of this technology in Brazil is not very different. Due to the advantages of the oil as an energy source (i.e. its low price), solar devices only received support during the late 1970s, when, in 1978, the Brazilian Association of Solar Energy (ABES) was created with regional offices in various states. This phase was of great improvement to the area for about ten years, when the studies were discontinued due to the, again, low funding and high prices. The period between the late 1980s and the early 1990s was marked by an abrupt decrease in funds to this area, leading to the extinction of various solar energy research groups [DHE05].

In 1994, Brazil received a great boost in the photovoltaic field, allowing the country to start laboratory development and production of solar devices. In 2004, the Brazilian Center for Development of Solar PV Energy (CB-Solar/NT-Solar) was created in the Pontifical Catholic University (PUC-RS) at Porto Alegre [DHE05][ZAN12]. The NT-Solar is the most modern and well-equipped photovoltaic development center in Latin America [DHE05].

The NT-Solar has a large physical area and several resources, as cleanroom facilities (10000 class [MOE12]), diffusion furnaces, photolithography, thin-film deposition, chemical processing, encapsulation, etc. [DHE05]. Fabricating good quality solar cells require all the previous listed equipment and processes. It can be fabricated through different ways, ending up in different results for each fabrication method. Anyhow, all of these fabrication paths are composed of chemical and physical reactions, and must be performed in a cleanroom to avoid external particles contamination.

Most of solar cells are fabricated using semiconductor materials, like gallium arsenide, germanium, silicon, etc. However, even not being the best option due to its low band gap (1.12 eV) and not so good response to light, silicon is the most used material in solar cells fabrication. The reason to explain this fact is that silicon is one of the most abundant elements in the Earth's crust.

The incidence of light over a photosensitive device like a silicon solar cell induce the generation of an electric current and a voltage differential. This event is called *photovoltaic effect*. Solar cells work using this principle, when a photon with the minimum required energy (higher than the band gap) penetrates into the solar device, an electron-hole pair (EHP) is created and separated by the p-n junction of the cell [WYS60]. In the case of a load connected to it, the electrons flow through that load and return to the cell, recombining with the holes again. This behavior causes the current to be created.

1.1 Motivation

Transporting, refining and burning are some steps taken to use oil as an energy source. Considering that all of them consume a high amount of energy, one should question seriously whether it makes sense to use more than a barrel of oil worth of energy to obtain and convert the energy available in a barrel of oil [MES00]. Based on this observation, as well as the known limitation of fossil fuels sources on the Earth, one may consider the solar energy as a strong alternative to solve the energy problem of the world. The only cost of generating electricity from a photosensitive device is the fabrication and storing, thus, the produced energy is clean [CHO00], non-residual and provided by the sun, an infinite power resource.

On 2013, the author had the opportunity of taking a course on photovoltaic systems in the United States through the program Science without Borders. Along this period, he was able to study and experience the technology, as well as fabricate four solar cell devices. On his return to Brazil, he saw the possibility of studying further the subject and the cells performances, especially among the current devices available in the industry scenario.

1.2 Objectives

The main objective of this project is studying the technology and evaluating the performances of the four solar cells fabricated by the author. To help on the achievement of this goal, this project focused on the accomplishment of the following items:

- Compile a solid and objective document about the solar cells technology, including its functional principles and the most efficient devices nowadays.
- Detail the fabrication processes used on the development of the four solar cells.
- Present the electrical characterization and analyze the performances of the solar cells mentioned in the previous item.
- Classify the fabricated devices performances among the current solar cells industry by comparing them to an existing industrial manufactured device.
- Define an application scenario for the developed solar cells.

1.3 Document Structure

This document is organized as follows. **Chapter 2** introduces the basic concepts necessary to understand the fabrication and characterization of solar cells. **Chapter 3** presents an overview on some of the most used techniques to fabricate solar cells. **Chapter 4**, state of the art of the solar cell structures, fabrication methods and the latest solar cells' efficiency records. **Chapter 5** details the process sequence used to fabricate the four solar cells. **Chapter 6** presents the characterization of the fabricated devices, compares them to an existing industrial manufacturing cell and proposes an application scenario. **Chapter 7** concludes the knowledge gathered in this project.

2 CONCEPTS

This Chapter presents the main concepts that need to be emphasized in order to understand solar cells functionality, fabrication and characterization factors.

2.1 Solar Cell Structure

The main idea (and most essential) of a solar cell is a conductible substrate doped with various elements of different electron orders, forming a p-n junction [LOR94]. Normally, the positive and negative connectors can be found at the cell's bottom and top, respectively. Also, an antireflection layer (Section 3.2.4.2), texturing (Section 3.2.2.1) or both, may be applied to avoid energy losses. The structure explained here can be visualized in Figure 1, which is the illustration of a silicon cell cross-section connected to a load. In this example, the p-n junction could be represented by the emitter being the n-type, and the base being the p-type.

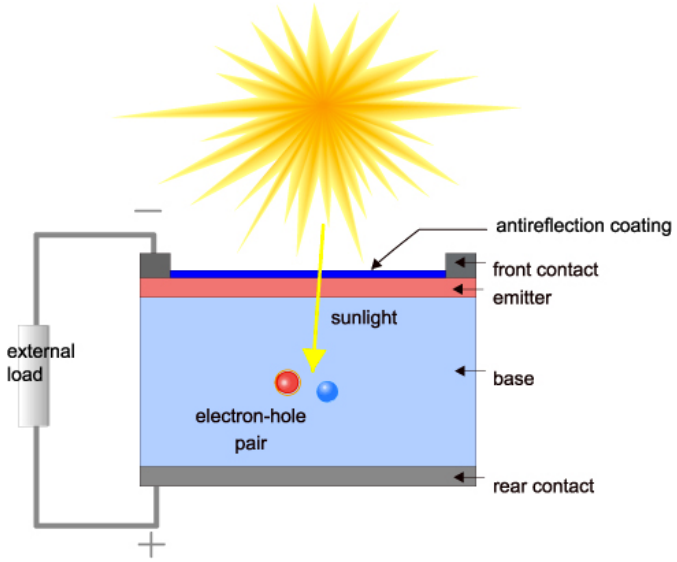

Figure 1 - Solar Cell cross-Section [PVC14].

2.2 Solar Cell Equivalent Circuit

The equivalent circuit of a solar cell (Figure 2) is composed by a current source controlled by the intensity of light, this means that, more light sourced, more current will be generated until reaching its maximum current point. To represent the voltage generation, an ideal diode is found in parallel to the source, displaying I_0 as its saturation current [LOR94] and the open-circuit voltage as the highest voltage achievable. The series resistance is placed in series with the output connector, as well as the shunt resistance is parallel to the current source, the diode and the load. All the cited circuit parameters and components are explained on the following Sections.

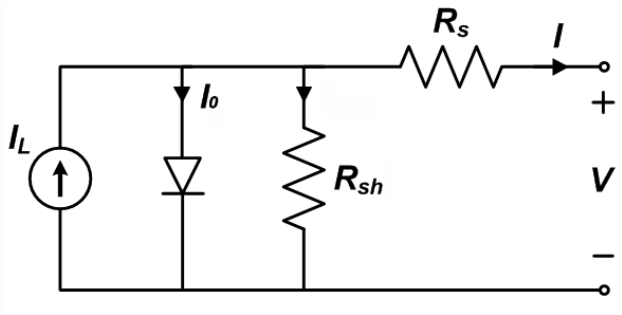

Figure 2 - Cell's equivalent circuit

2.3 Important Voltages and Currents

2.3.1 Dark Current

Photovoltaic devices, under no light have the same behavior of a diode with saturation current, named *dark current* (I_0). This current directly affects the cell's I-V curve since it is opposite to the circuit, lowering the open-circuit voltage (Section 2.3.3) and the Fill-Factor (Section 2.4) [BAI13][LOR94]. Normally, the natural potential difference between both contacts is the main reason for generating this current [LOR94].

2.3.2 Light Generated Current

Through the event of the photovoltaic effect, electrons and holes are created and then separated by the p-n junction, leaving the electrons at the n-side and the holes at the p-side. Having a load connected to the device's contacts allows the electrons to run through it and later recombine on the substrate, creating a *light generated current* (I_L). Equation 1 [LOR94] shows the behavior of the I_L together with the I_0, resulting in the actual *net current* (I) of the circuit.

$$I = I_L - I_0\left(e^{\frac{qV}{nkT}} - 1\right)$$

Equation 1 - Voltage over current relation

In Equation 1, q represents the electronic charge, V the voltage, n the ideality factor, k the Boltzmann constant and T the temperature in Kelvins.

2.3.3 Short-Circuit Current and Open-Circuit Voltage

The solar cell's I-V curve (Figure 3) presents the behavior of the current over the change in voltage. Two points in graph are essential to the characterization of a solar cell, the *short-circuit current* (I_{SC}) and the *open-circuit voltage* (V_{OC}).

The I_{SC} is the current at zero voltage [PVC14]. Some factors may be of a great influence to this current, like the solar cell's area, the number of photons arriving at the surface, the light spectrum (Section 2.8.1) and the cells' probability of photon collection [PVC14]. Although, when at open-circuit, the cells display no net current, but a voltage V_{OC}, which is the greatest voltage value possible to be presented by the cell, and can be calculated by Equation 2 [PVC14].

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{I_L}{I_0} + 1\right)$$

Equation 2 - Open-circuit voltage.

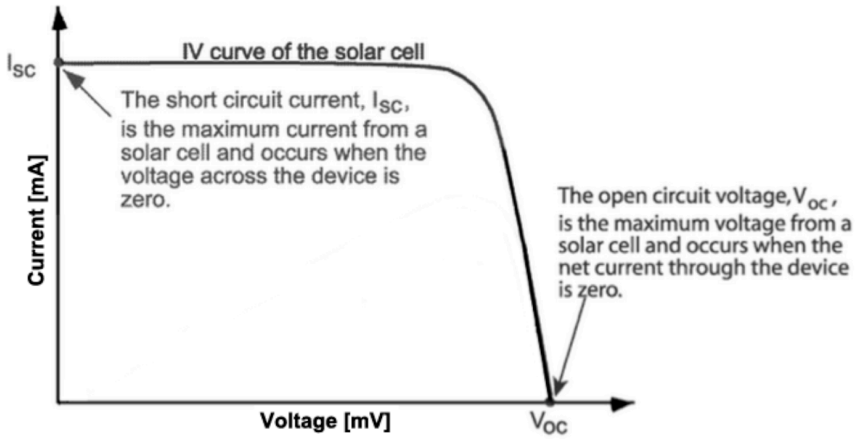

Figure 3 - Solar cell I-V curve [PVC14].

2.3.4 Maximum Power-Point

The *maximum power-point* (M_{PP}) is the greatest power value a solar cell can present (Equation 3). Figure 4 depicts a representation of this power point, where the red line represents the I-V curve of the cell, and the blue line the power represented by the red curve.

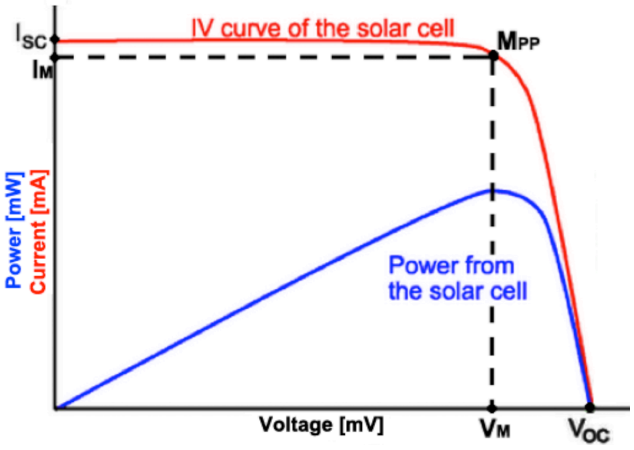

Figure 4 - I-V curve including M_{PP} [PVC14].

$$M_{PP} = V_M \times I_M$$

Equation 3 - Maximum power-point.

2.4 Fill Factor

The *fill factor* (FF) is a way to measure the quality of the cell. Solar cells with high internal resistance and great losses have low FFs. This parameter is obtained by the ratio between the area demarked by the M_{PP} and the one demarked by the $I_{SC}xV_{OC}$ point, as presented in Figure 5. For an ideal silicon solar cell, the fill factor would be considered to be 89% [SZL97]. Therefore, consider the Equation 4 [PVC14] to the calculation of the FF.

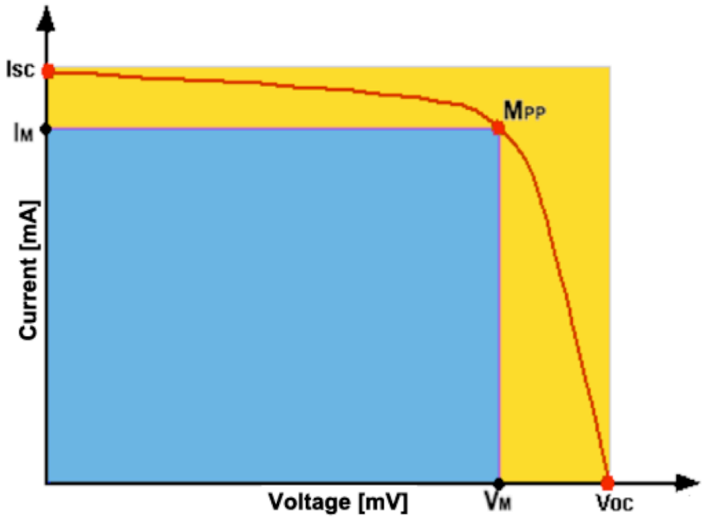

Figure 5 - Fill Factor [PVC14].

$$FF = \frac{V_M \times I_M}{V_{OC} \times I_{SC}}$$

Equation 4 - Fill Factor.

2.5 Efficiency

Efficiency (η) is the key factor considered in any photovoltaic project, and it is commonly used as a parameter to compare the performances of solar cells. Studies have shown that the ideal silicon solar cell would present the maximum efficiency of 29% at standard test conditions (the standard conditions will be treated in Section 2.8.2) [SZL97].

The factor η is defined as the ratio between the solar cell output and the *input power* (P_{in}) from the light source (Equation 5) [PVC14].

$$\eta = \frac{V_{OC} \times I_{SC} \times FF}{P_{in}}$$

Equation 5 - Efficiency.

2.6 Resistances

The cells may present some resistances along with their structures, some of them may be beneficial to improve the currents and voltages, but most of them directly diminish the device's performance. These are presented below.

2.6.1 Characteristic Resistance

The *characteristic resistance* (R_{CH}) is the ratio between the voltage V_M and current I_M. When this resistance is equal to the one in the connected load, the cell would be working at its maximum power-point [PVC14].

2.6.2 Parasitic Resistances

The intervention of resistive effects in solar cells results in a reduction on efficiency by dissipating power through resistances. The parasitic resistances, as they are defined, are the *series resistance* (R_S) and the *shunt resistance* (R_{SH}).

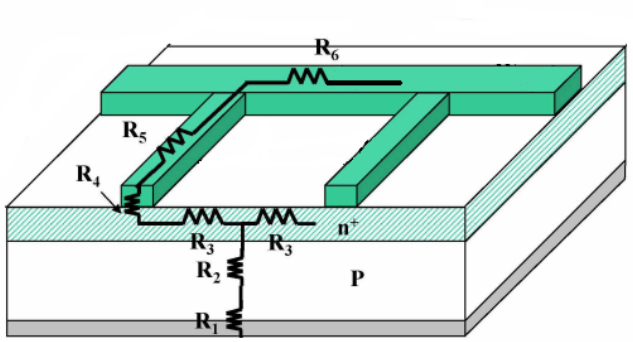

Figure 6 - Solar cell structure and the components that may cause the series resistance [EBO12].

The series resistance is mainly induced by the movement of current through the emitter and the base, and the resistances between the metal contacts and the substrate (see Figure 6). It is important to keep this resistance as low as possible to improve the cell's performance [MES00][PVC14].

Although, contrary to R_S, the shunt resistance is encountered in parallel to the cell diode (Section 2.2) and can represent a second path to the current to flow on the cell, decreasing the V_{OC} and the V_M. Since the idea for a good response of the cell is all the current flowing through the diode, R_{SH} must have a high value, and for ideal cells, almost infinite [LOR94].

These resistances directly influence the fill factor and efficiency. Figure 7 presents the effect of these resistances on the I-V curve, and indicates that, for a good performance of the solar cell, R_S must present a really low value and R_{SH} must present a really high value.

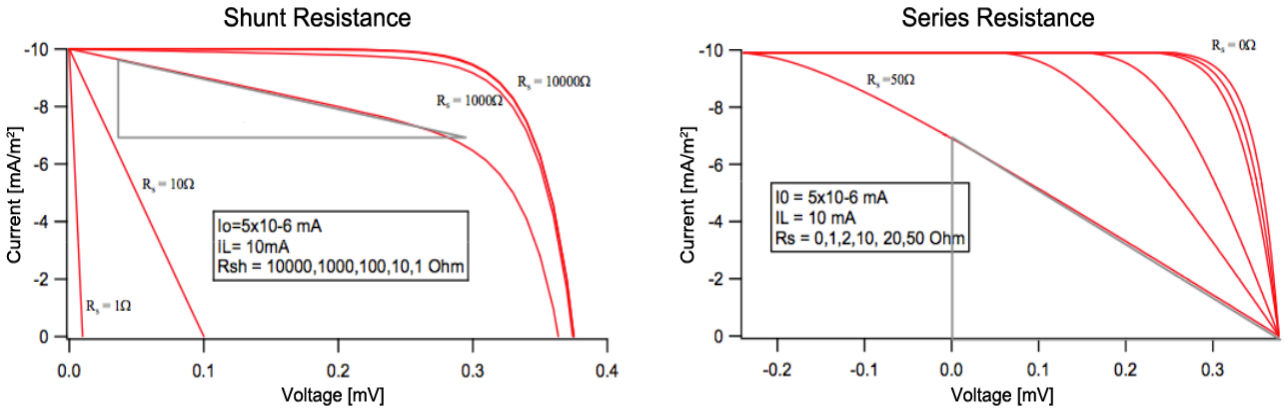

Figure 7 - The effect of the shunt and series resistances on the I-V curve [KAI14].

2.6.3 Physical Resistivity

During the fabrication process, some resistances may be taken into account in order to design a good cell. Lower values for theses resistances could lead to a better solar cell performance. A few of these are listed below (according to [PVC14]).

- Base (Bulk) Resistance – The resistance to the current flowed from the base to the top contacts.
- Emitter Resistance – The resistance of the emitter (n-type) of a standard cell structure.
- Contact Resistance – Resistance on the bond of the contacts to the substrate. To decrease this loss, normally, a heavy n-type dope is applied under the contacts.
- Finger Resistance – The finger contacts (Section 3.2.5) on the cell may display a power loss, which is directly linked to its length, width and spacing.
- Sheet Resistivity ($\rho_{\blacksquare}$) – It is directly linked to the ratio of the desired layer (measured layer) resistivity and its thickness, and it's normally expressed as Ω/□.

2.7 Effect of Temperature

Higher temperatures (higher than room temperature) have negative effects on silicon's band gap when compared to lower temperatures. An increase in temperature allows low-energy photons to create EHP, therefore, decreasing most of the device's parameters, especially the open-circuit voltage. Although, this increment in temperature increases the short-circuit current, which may occur due to the commented decrease in the band gap, and also, because of a greater diffusion length of the minority carries [LOR94]. Figure 8 shows the effect of temperature over a solar cell I-V Curve.

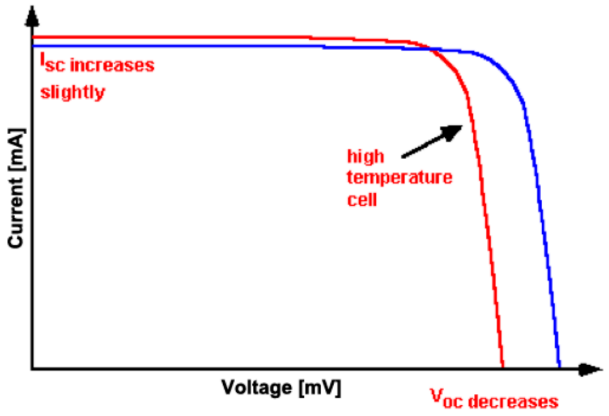

Figure 8 - Effect of temperature over a Si cell I-V curve [PVC14].

2.8 The Sunlight

2.8.1 Light Spectrum

The light as we see is only a small fraction of the total energy emitted by the sun. It is known that light has a wave-particle behavior, and, by the variation of the wavelength/frequency (Figure 9), it is possible to achieve different light colors and/or types. [PVC14].

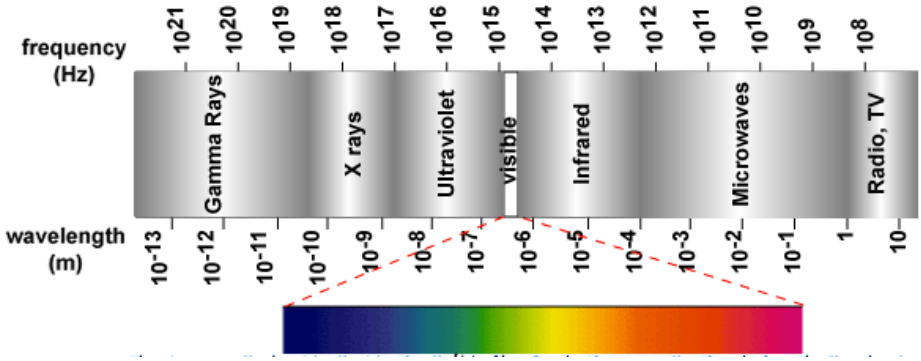

Figure 9 - Light spectrum [PVC14].

Photons need a minimum energy to create EHP in a Si solar cell. Figure 10 shows the spectral response of a Si cell to the variation of light wavelengths. It is possible to notice that blue light is the color with the highest amount of energy, while red light has the lowest. When increasing to violet light, EHPs are created too close to the surface, thus, recombining before the junction separates them (front surface recombination), resulting in energy and current losses. Meanwhile, decreasing to the red colored light, the generation of EHP is made too close to the bottom, also, far from the junction, therefore, they recombine before they get separated (rear surface recombination) [PVC14].

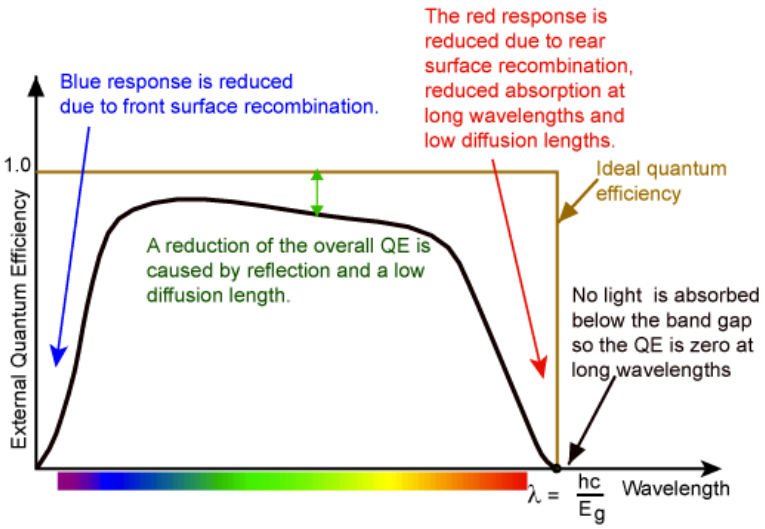

Figure 10 - Si cell spectral response [PVC14].

2.8.2 Solar Irradiance

The measure of power density of sunlight is the *irradiance* [W/m^2] and can be classified with an AM level, which means the *air mass* between a certain surface and the sun [AER69]. There are three classifications for these levels:

- **AM0 –** The energy constantly received by the Earth from the Sun at the top of the atmosphere, and is equal to 1353 W/m^2 [SZL97].
- **AM1 –** The energy, after passing the atmosphere, has its value is reduced to about 1000 W/m^2 (energy equivalent to 1-sun), which is fairly 28% less of AM0's magnitude [CRU05].
- **AM1.5 –** Can be divided in AM1.5G and AM1.5D, which means, global irradiance (direct and diffuse radiation [PVC14]) and direct irradiance, respectively. This classification represents the position of the sun begin exactly 45˚ above the horizon [SZL97]. It also presents an energy value equivalent to 1-sun, and is most commonly used to perform tests with terrestrial solar cells, therefore, it is the irradiance that will be used to test and characterize the devices in this project.

3 FABRICATION TECHNIQUES

This Chapter presents an overview on the different types of silicon crystallization and cuts, and the most used fabrication methods for solar cells.

3.1 Crystalline Silicon

Silicon is the most widely used material for the fabrication of solar cells due to its semiconductor behavior, and especially, to its high abundance on the Earth's crust. Silicon crystals can be classified according to the degree of crystal structure organization. These degrees are defined as *mono-crystalline*, *multi-crystalline, poly-crystalline* or *amorphous* [PVC14].

Mono-crystalline silicon (mono-Si) is the most used formation of the material on PV fabrication due to its solid and perfectly ordered crystal structure [LOR94]. The most common crystal growth techniques to this crystallization class are *czochralski* (cz-Si) and *float zone* (fz-Si). Also, because of its structure, mono-Si ingots can be cut in different directions according to the xyz-plan. These cuts are defined by the *Miller Index* (Figure 11), and can be recognized by the position of the flat on the finished wafer.

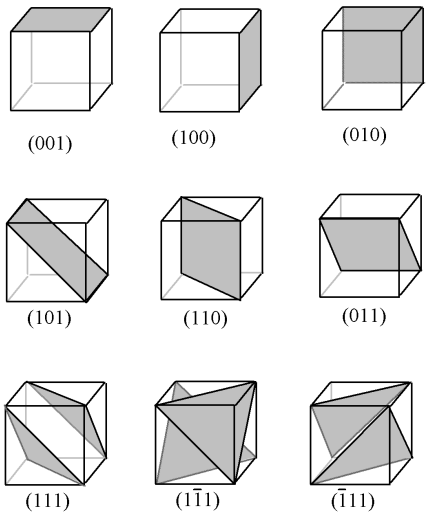

Figure 11 - Miller indices.

Since mono-Si is expensive when compared to other silicon crystal classes, multi-crystalline (mc-Si) silicon [PVC14] appear as an option to the fabrication of solar devices. The disadvantage of this material is that different fabrication methods may be used due to their non-regular atom structure [SZL97]. At last, there is the amorphous silicon (a-Si), which is classified as non-crystalline [SYA09] because of its small crystal grain sizes composition (smaller than 1 μm – μc-Si). It is commonly used on the fabrication of thin-film solar cells as mentioned on Section 4.2.1.

3.2 Fabrication Processes

The path for fabricating solar cells has different options, each of them leading to different efficiencies and costs. Figure 12 depicts an overview on the fabrication steps of a simple mono-Si solar cell through an industrial process composed of an etching step for saw damage removal and texturization, phosphorous diffusion, phosphorous silicate glass (PSG) removal, edge isolation, ARC deposition and screen-printed front and rear contacts [GOO13].

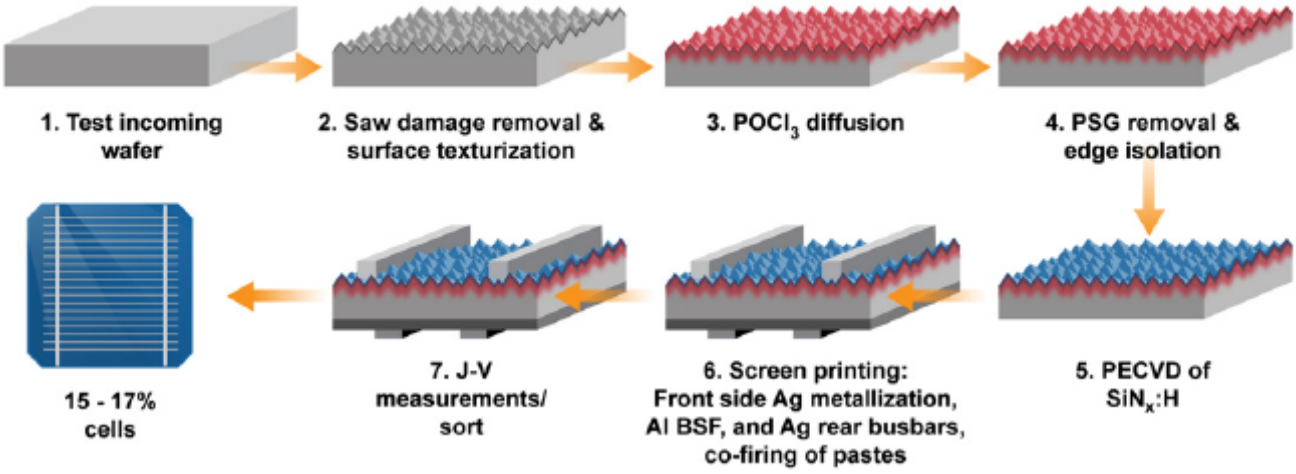

Figure 12 – Standard solar cell fabrication steps [GOO13].

The following processes describe different manners – including laboratorial and industrial – of fabricating solar cells (layers, junction, contacts, etc).

3.2.1 Photolithography

Photolithography has the purpose of transferring a defined pattern on a mask to the surface of the desired material through the exposure of light. This process is not widely used nowadays, especially in industrial manufacturing, due to its high costs and low wafer throughput. A single execution of the photolithographic process combines several different steps in sequence. These most commonly are: cleaning, barrier formation, photoresist application, soft-baking, alignment, exposure, development and hard-baking.

Firstly, the cleaning step is applied to clean the wafer of ionic, metallic or organic impurities. This is followed by the creation of a SiO_2 barrier over the wafer's surface as a protective layer. Then, it comes the photoresist application, which is applied on the center of the wafer that is placed on a spinning device to equally spread the solution over the surface. The photoresist, a ultra-violet (UV) sensitive chemical, can be either positive or negative. Positive photoresists will etch all the non-exposed locations of the wafer and the negative will etch only the locations exposed by the light through the mask.

After the photoresist application, the soft-baking process is performed to make the applied chemical more photosensitive. Later on, the wafer can be taken to a photolithography machine, where the alignment of the masks (if necessary) will be executed before the exposure to UV light. At last, the development step serves to dissolve the exposed resist by sinking the wafer on a chemical solution, and the hard-baking will harden and improve the adhesion of the remaining photoresist on the wafer's surface.

3.2.2 Etching and Cleaning

The etching process is normally described as the sinking of the wafers in a certain acid solution to etch a desired layer, improve the wafer's surface polishing (eliminate saw damaging from ingot sawing), and/or texturing [SEI83][GOO13]. In case of the cleaning step, it is normally applied after etching to remove the remaining etching solution, or even, in other situations, to remove undesired photoresist residues, metal, or organic contaminations.

3.2.2.1 Texturing

Etching is the easiest and cheapest method of texturing [SZL97]. Mono-Si with <100> orientation can be textured by an anisotropic etch at a temperature of about 75˚C in a solution of NaOH or KOH with the addition of isopropanol. This method produces pyramids randomly distributed along the wafer [KIN91]. These pyramids assist reducing the cell's reflection rate and allowing the increase of the *light-trapping effect* (photons getting trapped inside the substrate, reducing energy loss) [SZL97][KIN91]. Other texturing process for mono-Si, but not very cost- and time-effective [SZL97], is the application of a pattern through photolithography, followed by an etching, or the use of a special saw, to create the texture.

For mc-Si, the etching method can be slightly adapted to work with the non-regular characteristic of these materials, creating this texture with anisotropic chemical etches. Although, the most commonly used method, but only in laboratories, is the saw method, which uses one or multi mechanical saws to generate the texturing [SZL97][KIN91].

3.2.2.2 RCA Clean

The RCA clean process (a standard wafer cleaning process developed by the Radio Corporation of America [MOE12]) is the most used cleaning method for extermination of external contaminants. Normally, two steps compose this process SC1 and SC2, where SC stands for standard clean. The SC1 consists of a $NH_4OH/H_2O_2/H_2O$ mixture and has the purpose of removing the organic particles. Therefore, SC2 uses an $HCl/H_2O_2/H_2O$ solution, and aims the removal of metal contaminants [SZL97].

3.2.3 Forming the Junction

The junction of a standard solar cell is formed by a p-side and an n-side. The most used processes on the formation of the cell's junction are described as it follows.

3.2.3.1 Diffusion

The diffusion process begins with the deposition of a shallow high-concentration layer of the desired impurity on the substrate. At high temperatures (900 to 1200 ˚C), the impurity atoms move from the source into the silicon crystal. The diffused sources can be liquid, gas or solid [SEI83]. The gas type process is composed by the atoms' transportation through nitrogen between furnaces. The liquid type has the same process, but a previous evaporation is necessary. On the other hand, the solid type is normally a powder, which is heated separately and carried into the diffusion furnace, also, with the assistance of nitrogen [SEI83].

Another kind of solid dopant can be applied directly with the wafer in the furnace. It is another wafer, but instead of silicon, it is formed of the desired dopant (i.e. phosphorous or boron). When the furnace is heated, the atoms from these wafers, along with the help of nitrogen, are transported from its surface to the silicon's [SEI83].

3.2.3.2 Epitaxial Growth

This process is composed by the growth or deposition of crystals of the desired dopant on a single crystal wafer. The silicon's surface is etched as preparation, followed by the transportation of the wafers to a laminar flow station. Nitrogen is used to purge the epitaxial station and assist on the deposition (growing) of the junction at a suitable concentration level [SEI83].

3.2.3.3 Ion Implantation

Ion implantation method is basically composed of the acceleration of ions in an electric field, followed by the redirection of those ions through a vacuum to the wafer, as well as, their implantation into the lattice of the substrate [SEI83]. The wafer may be masked to lock the ions into specific areas; therefore, a photolithographic step may be needed prior to ion implantation.

3.2.4 Passivation Layers

To protect from external contaminants, reduce recombination and/or diminish the reflectance of light, among other characteristics, high efficiency solar cells have the deposition, or growth, of passivation layers on its fabrication process. Some structures presented on Chapter 4 can show more than one protective layer to improve efficiency.

3.2.4.1 Formation Techniques

- **Oxidation –** Thermal oxidation is the process of creating an oxide layer over the wafer's surface through heating. In case of silicon, the growth of a SiO_2 layer can be achieved by heating the wafer up to temperatures between 900 and 1200˚C, in an environment containing either pure oxygen (dry oxidation) or water vapor (wet oxidation).
- **Chemical Vapor Deposition (CVD) –** The CVD technique is a chemical process for depositing thin-films of various materials over the desired substrate. In a typical process, the substrate is exposed to one or more material sources, which react and/or decompose on the substrate surface by depositing the desired layer [ENG14]. There are many variations of this technique, and some of them are frequently used in the photovoltaics industry, for example, the plasma enhanced CVD (PECVD) [GOO13], the hot wire CVD (HWCVD) [MAT10], and others.

3.2.4.2 Anti-Reflective Coating

The *anti-reflective coating* (ARC) provides a certain protection to solar cells from reflecting the incident sunlight and also serves as a passivation layer. For research laboratory cells, the growth of an oxide followed by a deposition of ZnS and MgF_2 is a well-used method for creating an effective ARC [ZHA91]. On the other hand, in case of industrial solar cells, the deposition of SiN_x through (mostly) PECVD, is the most widely used solution to avoid light reflection [THO10]. Therefore, the surface passivation is effective and regularly leads to an improvement in the photo-generated current and open-circuit voltage [SZL97].

3.2.5 Metallization

The creation of front and backside metal contacts, also known as *metallization*, is one of the most important and expensive steps in the fabrication of solar cells [EBO12]. The front contacts (fingers and bus bar) are responsible for the gathering of electric energy along the solar cell, as well as an external connection

for current output. These contacts creation, if not well performed, results on the generation of shading losses and high resistances.

On the other hand, the *Back Surface Field* (BSF), the layer responsible for reflecting incident photons into the cell and preventing the rear surface recombination, is directly linked to the creation of the backside contact [PVC14], and can be created either by metallization or diffusion. Therefore, three of the most used methods for metallization, including advantages and disadvantages, are listed and explained below.

3.2.5.1 Metal Evaporation

For the application of the metal evaporation method (Metal PVD – Metal Physical Vapor Deposition), a photolithography must be applied to pattern the wafer in order to execute a metal deposition, especially in case of front contacts. This metallization process can be performed by three different ways: electron beam evaporation (EBE), sputtering or filament evaporation [SEI83].

In the EBE way, an electron beam heats the metal (normally Al or Ag) up to its evaporation, depositing it on the wafer's surface. In the case of the sputtering method, ions of inert gas are directed into a vaccumized chamber. Then, the ions are drawn to a target by RF (radio frequency) power and bounce into it expelling atoms (*sputtered atoms*), which are then deposited on the substrate. At last, in the filament evaporation process, a metal loop is connected between two filaments, having current running through it, increasing the temperature and melting. The metal evaporation is then deposited on the silicon wafers encountered inside the same chamber [SEI83].

This described metallization method is the most precise and efficient one nowadays. The use of photolithography allows the control of contacts sizes and metal depositions. On the other hand, the drawbacks of this process are the high costs and the need of a clean environment, thus, making it extremely impracticable in industrial manufacturing [EBO12].

3.2.5.2 Buried Contacts

The main idea of this method is creating holes in the substrate, generally using laser or mechanical scribers (See Figure 13). In most of the cases, to avoid recombination and energy losses, a diffusion step is necessary to cover the caved hole with a highly doped layer before depositing the metals [EBO12]. Later on, a deposition of Ni, Cu and a layer of Ag create the metal contacts [SZL97].

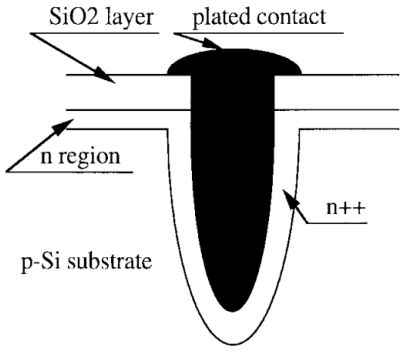

Figure 13 - Buried contact [SZL97].

The buried contact process can result in solar cells with low shading losses and good electric contacts. Also when compared to metal evaporation, this process is simpler. However, the industrial manufacturing has not adhered it yet, due to its considerable costs [EBO12].

3.2.5.3 Screen-Printing

The lack of really high temperature processes, the well fit to low quality materials (such as mc-Si or pc-Si) and the low-cost approaches allow that screen printing contacts turn to be the most used method in industrial manufacturing of solar cells [EBO12]. The process consists on the utilization of a printing machine, previously patterned with the contacts locations, that uses a paste consisting of metal powder, glass frit and organic binder [EBO12].

As temperature increases during contact co-firing, the organic binders burn out. Then the glass frit in the metal paste melts, etching the dielectric layer (ARC) underneath the gridlines, leaving only lead metal. The Plate metal dissolves into the melted lead, which dissolves the silicon subsequently. After the peak temperature, Ag precipitates and Si regrows such that the Ag is embedded beneath Si, creating a thin glass layer between the metals. For a better understanding, Figure 14 presents a zoomed picture of the finished printed contact [EBO12].

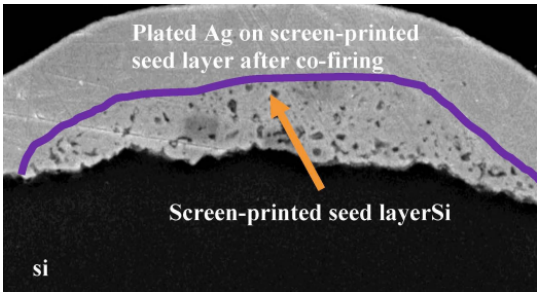

Figure 14 - Printed contact [EBO12].

3.3 Photovoltaic Module

The use of solar cells as an effective electric energy source requires the need of more than a single device. A whole PV *module* is composed of various solar devices, connected either in series or in parallel. Cells connected in series form a *string*, which are normally connected to each other, side by side (still in series), creating a kind of cell table. As shown in Figure 15, to create a PV module, the cell table is encapsulated and new layers are connected to its front and rear surfaces [PVC14].

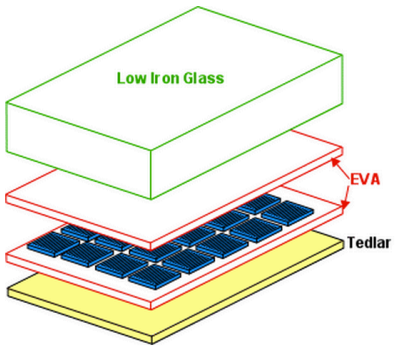

Figure 15 - Silicon module materials [PVC14].

In most cases, the front surface is composed of high light transmitting materials, like acrylic, plastic or glass. Generally, low iron-content glass is mostly used because of its low costs, strength, stability, transparency, water and gases impermeability, and its good self-cleaning properties. On the other hand, the

rear surface material is recommended to have a low thermal resistance and a great prevention against the ingress of water or water vapor. In most modules, a thin polymer sheet, typically Tedlar, is used [PVC14].

At last, *EVA* (ethyl vinyl acetate) is the most used material on the encapsulation of solar modules, providing adhesion between the solar cells, the top surface and the rear surface of the PV module. It should also be optically transparent and should have a low thermal resistance [PVC14].

4 State of the Art

This Chapter starts by presenting some of the most studied crystalline silicon (c-Si) research structures of solar cells, followed by examples of c-Si industrial manufactured devices, different and/or low-cost material options and the latest records on solar cells efficiencies.

4.1 Research Cells

Research cells seek for high efficiency devices and technology improvements, which, naturally, may come along with high costs [SZL97]. This Section presents two examples of research solar cell structures.

4.1.1 PERL Cell

The *passivated emitter and rear locally diffused* (PERL) cell, first developed by the University of New South Wales (UNSW), holds the record of the best small sized c-Si solar cell since 1999 – with the efficiency of about 24.7% using a fz-Si substrate [ZHA99] – and the second best of any size, losing only to the recent development of Panasonic [TOM14] discussed in Section 4.2.1.1.

This solar cell structure is composed of a double oxide layer on the top surface and another on the bottom, between the substrate and the Al-BSF. One characteristic that differs the PERL cell among other cells is the locally diffused back contacts, in other words, the oxide on the back have small gaps along the its distribution, allowing the connection of the substrate with the BSF, these gaps receive a local heavy boron diffusion to avoid recombination in those areas [ZHA90].

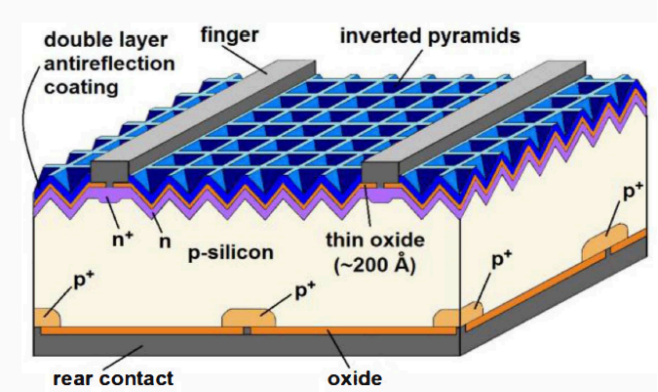

Figure 16 - PERL cell structure [ZHA90].

The front and back layers fabrication process of PERL cells is the photolithography, a method that can provide very low contact resistance, high efficiency and long-term stability. Therefore, the major advantage of PERL cells is the oxide layers, which create a solid passivation over most of the cell front and back surfaces, raising V_{OC}, I_{SC}, and the FF [ZHA99]. In addition, the *passivated emitter solar cell* (PESC), the *passivated emitter and rear contacts* (PERC) and the *passivated emitter and rear totally diffused* (PERT) are some variations of the presented structure [EBO12].

4.1.2 IBC Cell

The *interdigitated back contact* (IBC) solar cell is another structure resulted from the photolithography process. The main physical characteristic of the IBC cell is the non-existence of front contacts. The p-n junction is found at the bottom of the cell, together with the BSF. Both the positive and negative contacts are located at the same side. This way, the top of the cell is free of metals, reducing drastically the shading losses, the series resistance and recombination losses [EBO12]. Figure 17 depicts the explained structure.

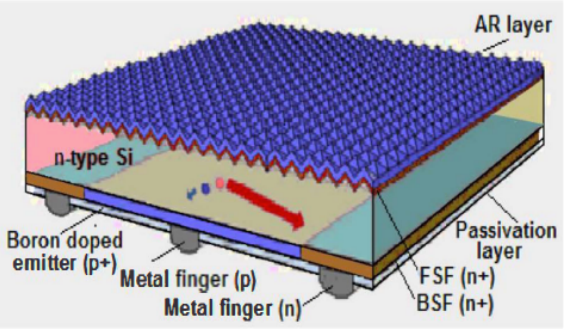

Figure 17 - IBC cell structure [EBO12].

In 2010, *SunPower Corp.* (owner of the structure rights) has demonstrated the efficiency of 24.2% on an n-type cz-Si wafer with 155.1cm^2 area. The implementation of high-passivated contacts and an optimized structure layout were the most important improvements to achieve the efficiency descripted [COU10].

4.2 Industrial Manufacturing Cells

Efficiency is not the only parameter targeted by the solar cell industry, costs are also taken into account. The industrial manufacturing of solar cells aims to balance costs and efficiency during devices fabrication. Low-cost materials and processes are preferred when they can, together, bring a reasonable and satisfactory efficiency rate. This Section presents some examples of industrial manufacturing solar cells, including two structure processes fabricated in PUCRS.

4.2.1 HIT Cell

The *heterojunction with intrinsic thin-layer* (HIT) cell, developed by *Sanyo Electric Co.*, is another well-known research solar cell model and one of the most promising structures that enables both high efficiencies and low costs. The main characteristic of this model is the existence of one or more i-Si layers on its composition. Also, its symmetrical structure and low temperature processes suit perfectly with the use of thin silicon wafer substrates [TAG14].

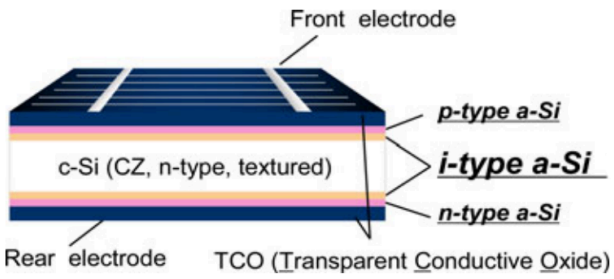

Figure 18 - HIT cell structure (Adapted from [TAG14])

The example shown of a HIT solar cell on Figure 18, developed by Sanyo on 2013, has presented a light conversion efficiency of 24.7% under 1-sun AM1.5 [TAG14]. Its p-n heterojunction is composed of a p-type a-Si layer and an intrinsic a-Si layer, deposited through PECVD, over a randomly textured n-type cz-Si wafer, while an intrinsic a-Si layer and an n-type a-Si layer compose the BSF of the cell by being deposited on the opposite side of the device. Also, both at the top and bottom of the structure, a transparent conductive oxide (TCO) layer and metal electrodes are placed to ensure a high conductivity, optimized pitch and low finger resistances [TAG14].

4.2.1.1 Interdigitated Back Contact HIT Cell

In 2013, *Panasonic Corp.* (the current owner of *Sanyo Electric Co.*), have developed a HIT solar cell presenting a light conversion efficiency of 25.6% under 1-sun AM1.5, considered the highest efficiency on silicon solar cells up-to-date. Figure 19, presents the structure of this latest achievement on the c-Si solar cells technology [TOM14][PAN14].

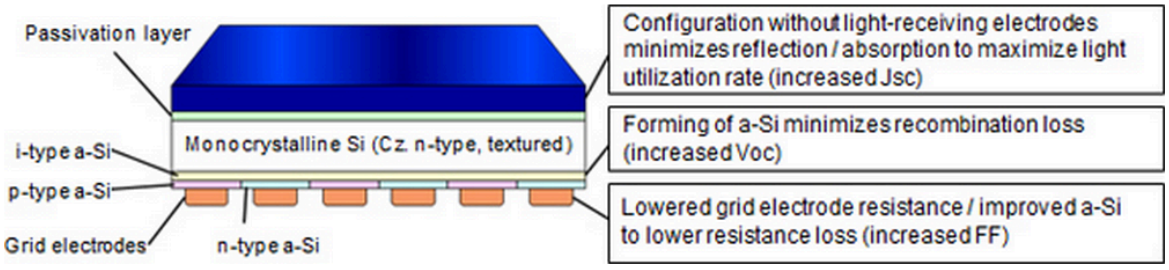

Figure 19 - Panasonic IBC-HIT cell [PAN14].

The placement of all the solar cell's contacts on the back, resembling the *SunPower* IBC cell, is the greatest improvement on this HIT structure. It is possible to notice on the image above that the p-n junction is totally made by the deposition of a-Si, even being a common characteristic of HIT cells. Also, the fact of all contacts being on the same side generates a great improvement on V_{OC} by the reduction in recombination. Thus, for the same reason, beyond diminishing recombination losses, this solar cell structure presents a great reduction on optical losses and resistance losses.

4.2.2 Industrial Cells at PUCRS

The solar cell industry in Brazil is not very wide. The country receives a large annual amount of solar radiation, but the photovoltaic technology has not been the first option as a renewable energy resource [MOE12]. One great improvement on this area in Brazil was the creation of the NT-Solar (CB-Solar), a well equipped laboratory center, inside the PUCRS campus at Porto Alegre [ZAN12]. The availability of this infrastructure allowed researchers and developers of the technology to perform experiences and projects.

Using the available resources, a pilot production of silicon solar cells and modules using industrial techniques was started in 2012 by Moehlecke *et al.*, being the first completed production line (from cells to module) to ever be performed in a university campus in Brazil. During this project, two process sequences were followed, creating n^+pn^+ and n^+pp^+ solar cells. Both structures were fabricated using a p-type cz-Si, <100> orientation and 300μm thick wafer substrate and characterized under standard conditions (1000 W/m^2 at AM1.5G and 25˚C) [MOE12]. The following two subSections present the fabrication and characterization of the two structures developed in the pilot project.

4.2.2.1 n^+pn^+ Cell

The n^+pn^+ solar cell process described in Figure 20(a) is based on a texturization etch with KOH solution, RCA cleaning, phosphorous diffusion using a $POCl_3$ source, phosphorous silicate glass removal, RCA cleaning one more time, TiO_2 ARC deposition, screen printing of the metal grid on the top and bottom with Ag and Ag/Al, respectively, and finally, a laser edge isolation to avoid external contact between top and bottom through the edges. The cross-Section on Figure 20(b) presents the organization of each deposited layer on the cell [MOE12].

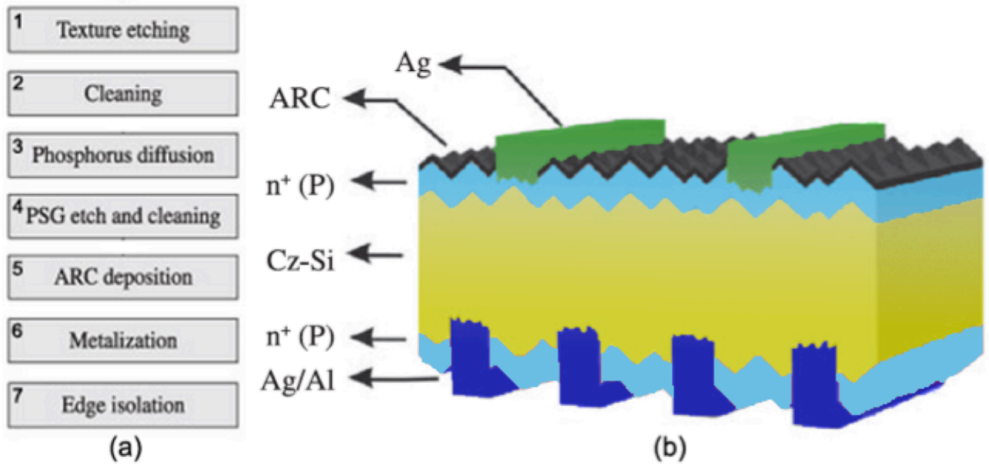

Figure 20 - n^+pn^+ (a) fabrication process sequence and (b) solar cell cross-Section [MOE12].

It is interesting to notice that, the deposition on both sides of the substrate with phosphorous creates a double p-n junction. Also, the ARC and the texturization diminish the reflectance of photons and improve light trapping. TiO_2 was used instead of SiN_x (as established in Section 3.2.4.2) because a high purity silane supply chain was not available in Brazil at the time [MOE12].

After the complete fabrication, tests could be performed to analyze their efficiency and other parameters. The actual average efficiency was measure to be around 12.7%, and *Cell 1* has presented the best efficiency over all – 13.4%. Modules were later built using these solar cells, and the average efficiency achieved was about 10% [MOE12].

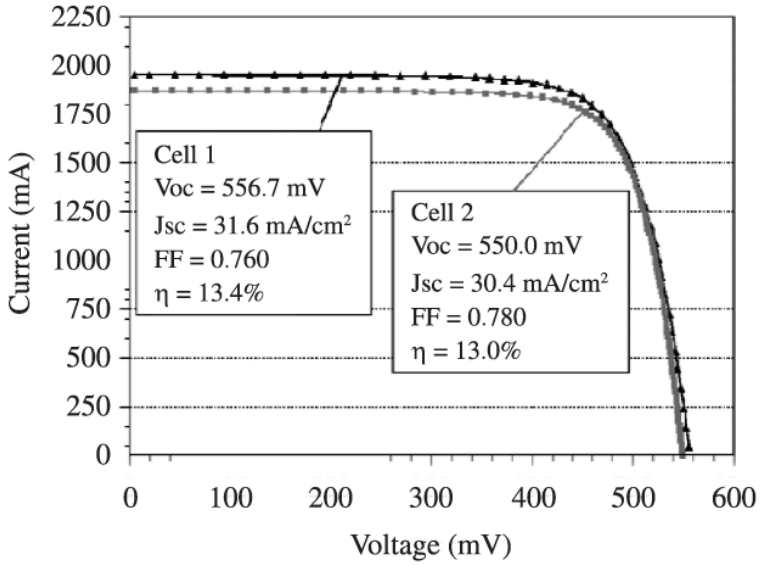

Figure 21 - n^+pn^+ characterization I-V curve [MOE12].

4.2.2.2 n^+pp^+ Cell

The solar cells using the n^+pp^+ structure were fabricated through the steps presented in Figure 22(a), resulting on a device with the cross-Section depicted by Figure 22(b). The fabrication started by a texturization etch with KOH, an RCA cleaning, the oxide (SiO_2) growth and etching on the top surface, another RCA cleaning, phosphorous diffusion, PSG removal, chemical cleaning, aluminum deposition and diffusion, TiO_2 deposition (ARC), screen-printing of the top and bottom contacts with Ag and Ag/Al, respectively, and a laser edge isolation [MOE12].

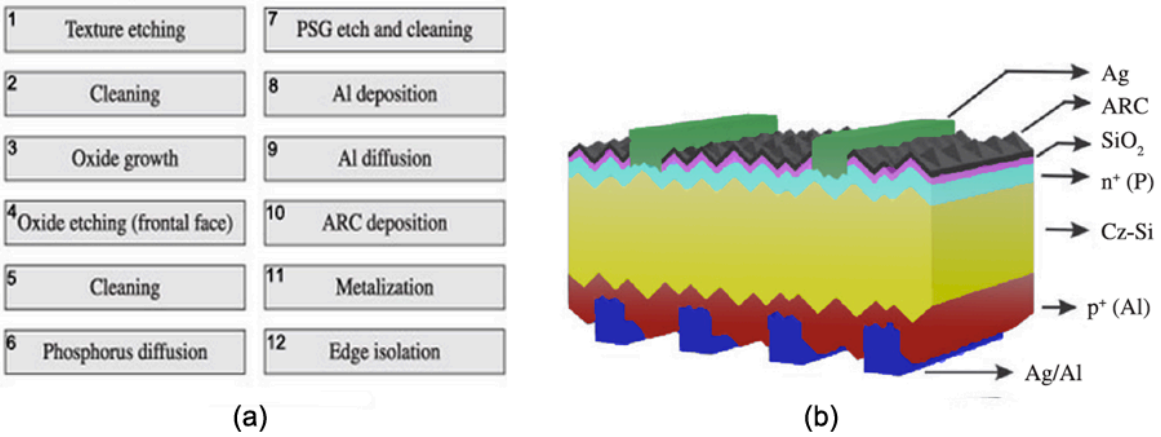

Figure 22 - n^+pp^+ (a) fabrication process sequence and (b) solar cell cross-Section [MOE12].

The process used on these cells was fairly complicated when compared to the n^+pn^+, the addition of an oxide layer and an aluminum layer on the back have added new steps to the fabrication process. On the other hand, the deposition of the Al layer on the back has created a back surface field that is meant to avoid bottom recombination and increase the values of the I_{SC} and the V_{OC}.

On Figure 23, the action of the BSF is notable when compared to the results of the n^+pn^+ structure. On the n^+pp^+ solar cells, all the parameters have increased, and the maximum efficiency achieved was of 16.1%, with a total average of approximately 14.5%. The modules later built with these cells have presented an average efficiency of about 12.1% [MOE12], which is still grater than the one presented on the previous Section.

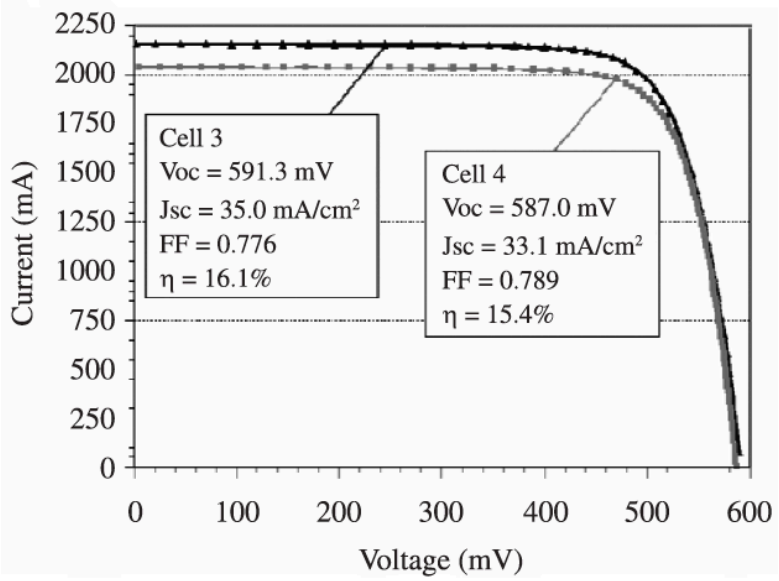

Figure 23 - n^+pp^+ characterization I-V curve [MOE12].

4.3 Structures Comparison

This Section presents on Table 1 a comparison between the advantages and disadvantages of each structure introduced on Sections 4.1 and 4.2.

Table 1 - Presented structures comparison.

	Advantages	Disadvantages
PERL	▪ High-Efficiencies [EBO12]. ▪ Locally diffused rear contacts to avoid rear recombination [ZHA90]. ▪ Low contact resistance [ZHA99]. ▪ Long-term stability [ZHA99].	▪ High-costs for materials and infrastructure [EBO12]. ▪ Unavailability of mass production due to difficult alignment and increased costs [EBO12].
IBC	▪ High efficiencies [BUN06]. ▪ Thinner cell [SZL97]. ▪ No contacts on the top, reducing shading losses. ▪ Positive and negative contacts on the same side, making it easier to interconnect for module assemble [PVC14]. ▪ Lower costs for materials and infrastructure [GOO13].	▪ Photolithography is necessary, thus, increasing costs. ▪ fz-Si substrate present a high minority carries lifetime.
n^+pn^+	▪ Low-cost fabrication. ▪ Fast and simple fabrication process.	▪ No BSF, which increases recombination [MOE12]. ▪ Below-average efficiency when compared to other industrial cells.
n^+pp^+	▪ Low-cost fabrication. ▪ BSF increases V_{OC} and I_{SC}, thus, the efficiency [MOE12]. ▪ Considerable efficiency for an industrial cell.	▪ A little more complicated process when compared to the n^+pn^+ [MOE12].
HIT	▪ High efficiencies. ▪ Reasonable low-costs [TAG14]. ▪ Bifacial structure [GOO13]. ▪ Simple and Low temperature processes [GOO13][TAG14]. ▪ Excellent surface passivation [GOO13].	▪ Increase in shading losses [TAG14]. ▪ Considerable resistive losses [TAG14]. ▪ Low temperature metallization can be quite expensive [GOO13].
Panasonic IBC-HIT	▪ Highest efficiency up-to-date [PAN14][TOM14]. ▪ Low recombination and resistance losses [PAN14]. ▪ Minimum shading losses due to no topside contacts [PAN14].	▪ Only achieved on laboratory [PAN14].

4.4 Multi-Junction Cells

Multi-junction solar cells, or *tandem cells*, are PV devices composed of multi-layers of different band gaps, mostly III-V materials [PVC14]. The fact of having this characteristic allow these kinds of cells to be able capture a higher range of light wavelengths, therefore, having the theoretical potential of achieving high conversion efficiencies of over 50% [YAM11]. Due to high efficiencies and great resistance against radiation, multi-junction solar cells have been widely used for space applications for many years [STA03].

On 2013, *Sharp Corp.* made the latest great achievement on this technology with the creation of an inverted 3-junction solar cell presenting 37.7% efficiency under 1-sun AM1.5G, and the impressive efficiency of 44.4% under concentrated sunlight (400 to 600-suns). These efficiency values represent, respectively, the highest efficiency ever achieved for a triple-junction solar cell, and the highest efficiency ever achieved by any solar cell under concentrated sunlight [SAS13]. Latest reports have indicated that *Soitec* may have achieved a 44.7% efficiency rate with a 4-junction solar cell under 297-suns, but no published information was found [SOI14].

Figure 24 shows the idea of the InGaP/GaAs/InGaAs inverted triple-junction solar cell fabrication process. Cell layers are grown by the metalorganic CVD (MOCVD) method over a GaAs substrate. After the full growth, the substrate is etched off and the layers are inverted and deposited over a silicon substrate by metal bonding. Later on, an MgF_2/ZnS ARC is formed over the solar cell before the metallization. This cell presents an optimized structure and contact grid layouts, resulting in a really low series resistance [SAS13].

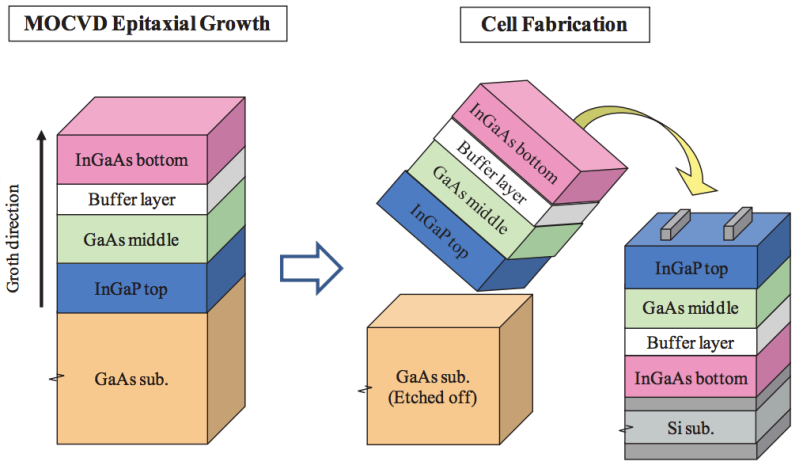

Figure 24 - Schematic view of the structure fabrication [SAS13].

4.5 Low-Cost Material Cells

One approach to reduce the solar devices costs is the use of low-cost materials as substrates (like stainless steel, graphite, ceramic or even glass) deposited with a thin layer (30-50µm) of amorphous silicon. The Silicon-Film™ process (Figure 25) is one example of low-cost PV cells production. This structure is composed of a metal BSF, followed by a low-cost ceramic material substrate, a metallurgical barrier, a p-type pc-Si layer and the top metal contacts [SZL97].

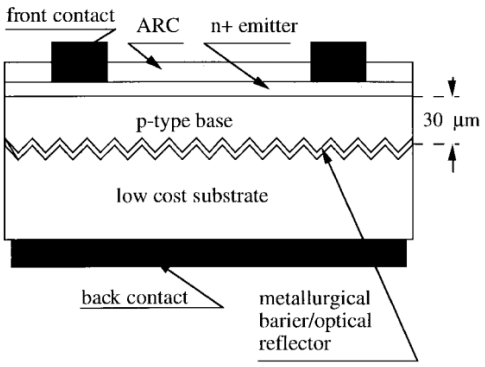

Figure 25 - Silicon-Film™ structure [SZL97].

The metallurgical barrier is texturized, serving as a light trapping and a reflector, also, protecting the thin silicon layer from the ceramic's impurities. Since the silicon sheets are fabricated at a desired thickness, ingot sawing is not necessary, leading to a notable cost reduction. Therefore, studies showed that a cell fabricated through this process with an area of 675cm^2 has presented an efficiency of 11.6% (test scenario was not provided) [SZL97].

4.6 Organic Cells

Organic materials, like polymer, can also be used to manufacture solar cells, presenting low costs and the possibility of creating flexible devices. An impressive example of these materials is the OMeTAD, which studies have presented great photo-induced charge-carrier conversion efficiencies [BAC98]. Most of the organic materials that have been studied lately have networks composed by fullerene, which is a non-natural carbon formation (C_{60}) with high conduction characteristics, and a possible substitute to silicon [CRU05].

Another example of organic compounds on solar devices is the dye-sensitive cell. These PV cells are a hybrid of organic and inorganic materials that have a relatively simple and inexpensive manufacturing process. Hybrid materials, especially the n-type TiO_2 cells, present the advantage of having its electron transportation due to the majority carries, different from silicon, which is due to the minority [CRU05].

Since the conventional solar cell materials are quite difficult to acquire in Brazil, even being one of the greatest silicon producers worldwide, organic solar cells, especially the dye-sensitized ones, come as an interesting option of study. These materials present low-costs, easy fabrication and long-term stability comparable to silicon. Also, Brazil enjoys all the necessary materials for the fabrication of these structures, but, so far, the dye-sensitized solar cells still remain with really lower efficiencies when compared to the silicon-based solar cell technology [DUA12].

4.7 High-Efficiency Solar Cells

This Section presents the highest efficiencies recorded on solar cells up to May 2014. It starts with Figure 26 graphically illustrating all the top solar cell structures and efficiencies since the late 70s up to now. Following, Table 2 highlights the current highest efficiencies measured under 1000W/m^2 AM1.5G at a cell temperature of 25˚C.

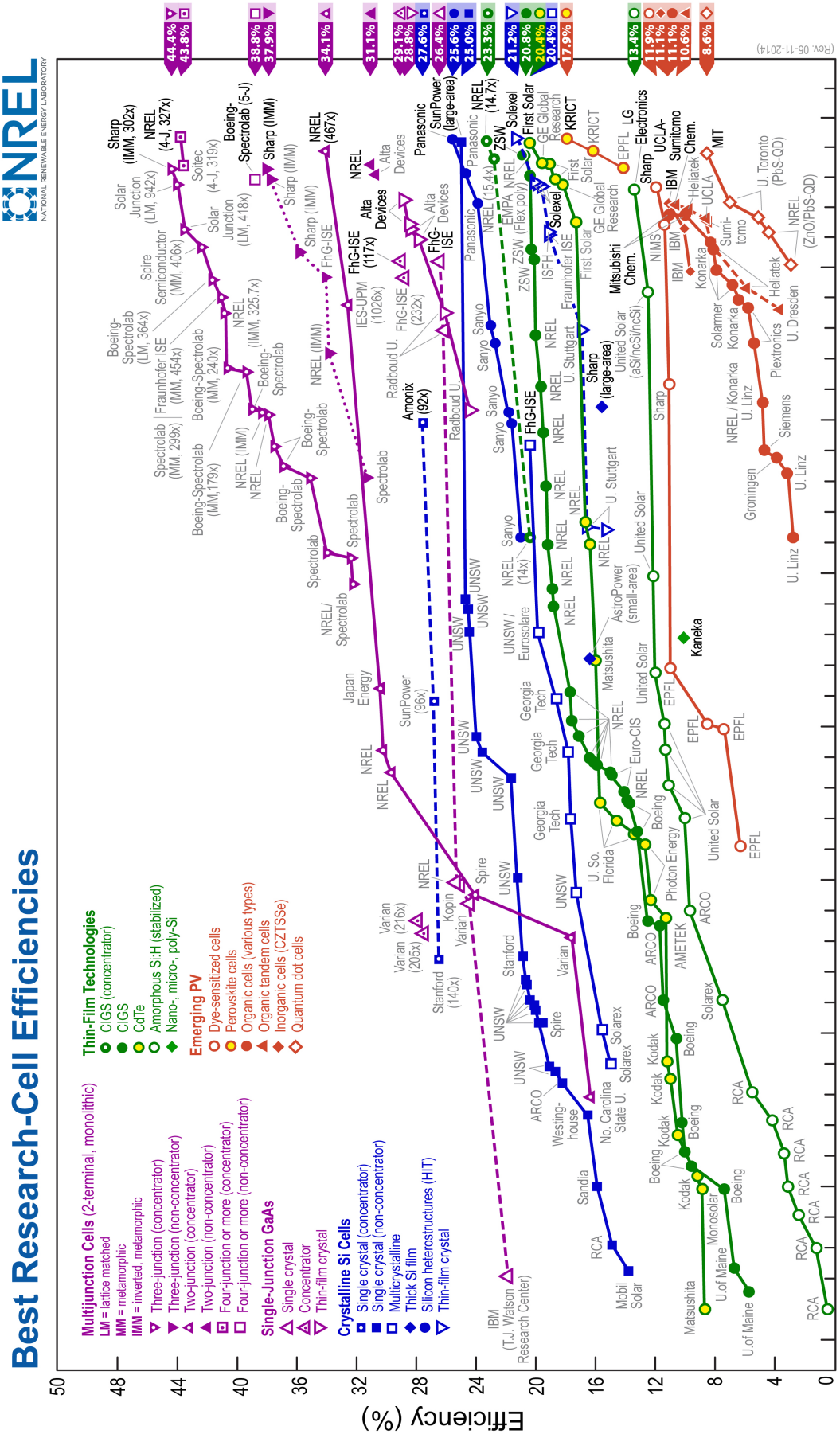

Figure 26 - NREL best research cells [NRE14].

[1] The highest Si cell single crystal (non-concentrator) measurement do not agree with the published paper by *SunPower Corp.*, which define the efficiency as 24.2%, thus, keeping the UNSW PERL cell as the highest efficiency achieved for this category [COU10].

[2] According to the publications of *Sharp Corp.*, the efficiency of 44.4% achieved by the IMM Three-junction (concentrator) was with the light intensity of 400 to 600-suns, not 302-suns as defined above [SAS13].

[3] About the CIGS Thin-Film and the dye-sensitized cells: no published information was found to support the defined efficiencies.

Table 2 - Terrestrial measure of solar cells efficiencies under 1-sun AM1.5G up to May 2014.

Classification	Efficiency (%)	Area [1] (cm^2)	Fill Factor (%)	Test Centre [2] (date)	Description
Silicon					
Si (c-Si) [3]	25.6	143.70	82.7	AIST (4/14)	Panasonic HIT
Si (mc-Si) [4]	20.4 ± 0.5	1.002 (ap)	80.9	NREL (5/04)	FhG-ISE
III-V cells [4]					
GaAs (thin-film)	28.8 ± 0.9	0.9927	86.5	NREL (10/12)	Alta Devices
GaAs (multi-crystalline)	18.4 ± 0.5	4.011 (t)	79.7	NREL (11/95)	RTI, Ge Substrate
InP (crystalline)	22.1 ± 0.7	4.02 (t)	85.4	NREL (4/90)	Spire, epitaxial
Thin-Film Chalcogenide [4]					
CIGS	19.8 ± 0.6	0.9974	79.2	NREL (11/13)	NREL, on glass
CdTe	19.6 ± 0.4	1.0055	75.6	Newport (6/13)	GE Global
Amorphous/multi-crystalline Silicon [4]					
Si (a-Si)	10.1 ± 0.3	1.036 (ap)	67.8	NREL (7/09)	Oerlikon Solar Lab.
Si (μc-Si)	10.8 ± 0.3	1.045 (da)	73.2	AIST (9/13)	AIST
Dye Sensitized [4]					
Dye Sensitized	11.9 ± 0.4	1.005 (da)	71.2	AIST (9/12)	Sharp
Organic [4]					
Organinc thin-film	10.7 ± 0.3	1.013 (da)	68.9	AIST (9/12)	Mitsubishi Chemical
Multi-Junction Devices [4]					
5J GaAs/InP bonded	38.8 ± 1.9	1.021 (ap)	85.2	NREL (7/13)	Spectrolab 5
InGaP/GaAs/InGaAs	37.9 ± 1.2	1.047 (ap)	86.7	AIST (2/13)	Sharp
a-Si/nc-Si/nc-Si (thin-film)	13.4 ± 0.4	1.006 (ap)	71.9	NREL (7/12)	LG Electronics
a-Si/nc-Si (thin-film cell)	12.3 ± 0.3	0.962 (ap)	69.4	AIST (7/11)	Kaneka

[1] (ap), aperture area; (t), total area; (da), designated illumination area.

[2] FhG-ISE, Fraunhofer-Institut für Solare Energiesysteme; AIST, Japanese National Institute of Advanced Industrial Science and Technology; NREL, National Renewable Energy Laboratory.

[3] Data taken from [PAN14] and [TOM14].

[4] Data taken from [GRE14].

5 Fabrication Development

This Chapter presents a detailed description on the development of the solar cells. The devices were fabricated at the Montana State University (MSU) cleanroom facilities, in the city of Bozeman, Montana, United States. The photolithography processes were ran on a 1500 sq. ft. class 1000 cleanroom, while the other processes occurred on class 10000 cleanrooms of 500 and a 200 sq. ft.

Figure 27 illustrates the steps used to fabricate the four solar cells studied in this project. These devices were fabricated through a mixture of thin-film and bulk silicon processing techniques. The wafer diameter was 100mm, 525±25µm thick, <100> orientated, single-side polished, single-crystal cz-Si, doped with boron (p-type) to a resistivity of 1-10Ω-cm.

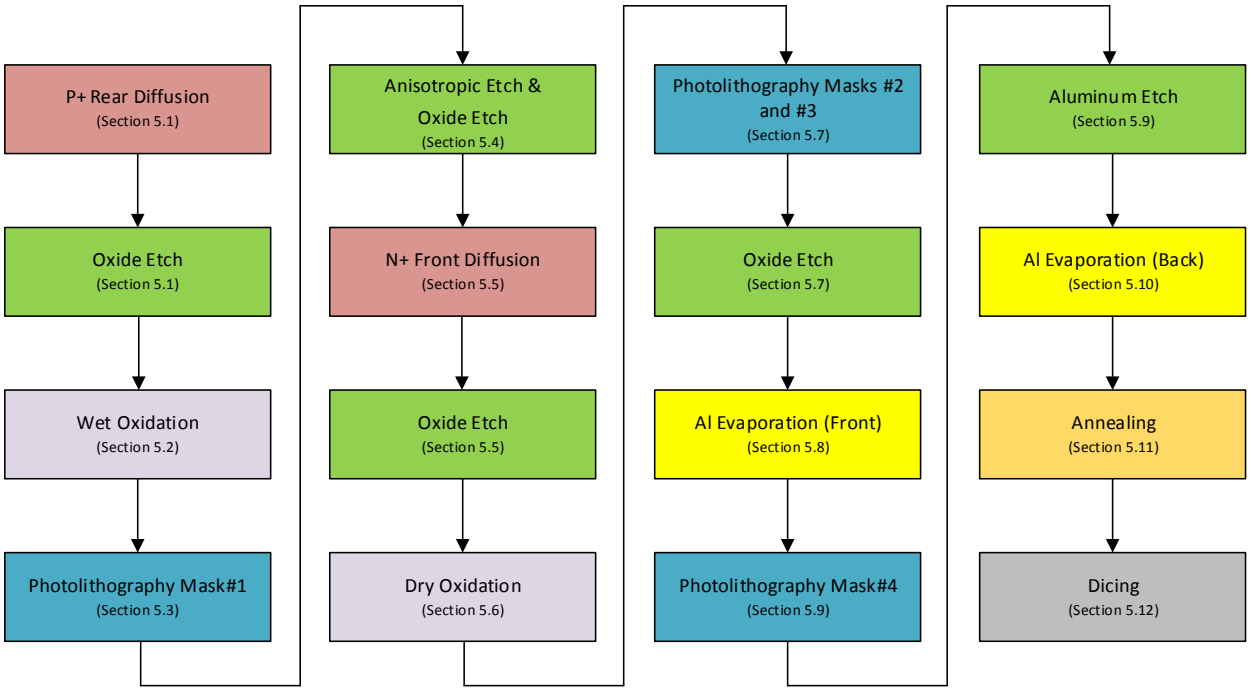

Figure 27 - Process flowchart overview.

The following Sections detail each step presented above, including the time, temperature and chemical solutions. The resistivity, oxide thickness and aluminum thickness are also monitored.

5.1 P+ Rear Diffusion & Oxide Etch

The fabrication starts with a boron diffusion to the back of the wafer. This process will create a p^+ layer on the back surface, forming a BSF that serves as a passivation layer, diminishes the solar cell rear surface recombination and improves the contact to the later inserted aluminum contact.

Figure 28 - Wafer with the p+ layer [KAI09].

The diffusion process used a solid Br dopant applied directly with the wafer into the furnace. The wafer was positioned on a quartz boat interspersing the silicon wafer and the boron sources (the backside turned to the Br wafer). Therefore, in a temperature of 950˚C during 50 minutes in the boron diffusion furnace, the Br atoms move out of the source wafer and deposit themselves onto the wafer's surface with the assistance of nitrogen, which is being pumped into the furnace during the process. The images below illustrate this diffusion process.

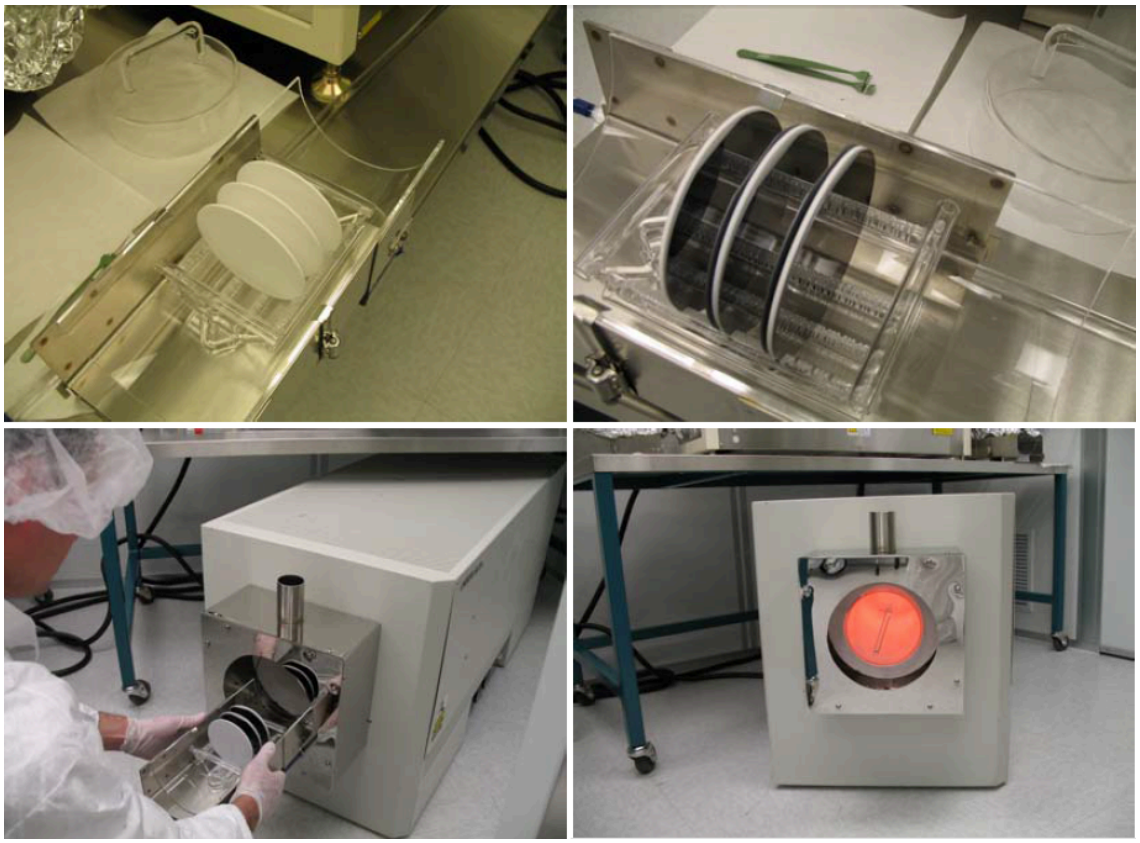

Figure 29 – Boron diffusion process [KAI09].

The diffusion of boron to the wafer's surface creates a borosilicate glass layer that needs to be etched off before continuing with the fabrication. To remove this layer, the wafer was submerged into a corrosive solution called 6:1 BOE (buffered oxide etch) for approximately 3 minutes. The 6:1 BOE solution is composed of one portion of water for every six portions of NH_4F, and has an etching rate of about 0.09 microns per second.

After the diffusion, the backside of the wafer developed a high conductive p^+ layer. The sheet resistivity of this new layer was measured using a *four-point probe* (Figure 30) to apply a current of 100μA to the wafer, which resulted in a resistivity of 194.3Ω/□.

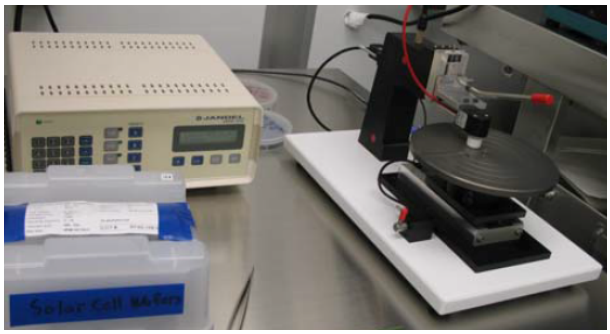

Figure 30 - 4-point probe used to measure the resistivity [KAI09].

5.2 Wet Oxidation

The role of the oxidation process is to create a SiO_2 layer of roughly 0.5µm thick around the substrate to later protect the wafer during the texturing process. The wafer was loaded on a quartz boat, having two dumb wafers on each end to maintain uniformity on the oxide layer. By using an oxidation furnace at a temperature of 1000˚C during 90 minutes, water vapor was pumped into the furnace with the assistance of an external bubbler. This vapor, in contact with the silicon wafer, started the creation of the SiO_2 layer.

Figure 31 - Wafer after the oxidation process [KAI09].

To ensure that the oxide layer was grown as expected, the thickness of the layer was measured using the *ellipsometer* presented in Figure 32. The measurement resulted in an oxide thickness of 0.43µm, which is close to the desired 0.5µm.

Figure 32 - Ellipsometer [KAI09].

5.3 Photolithography Mask#1

The role of the first photolithography is to pattern the mask#1 onto the wafer's surface in order to create gaps in the SiO_2 layer to perform later the texturization etch.

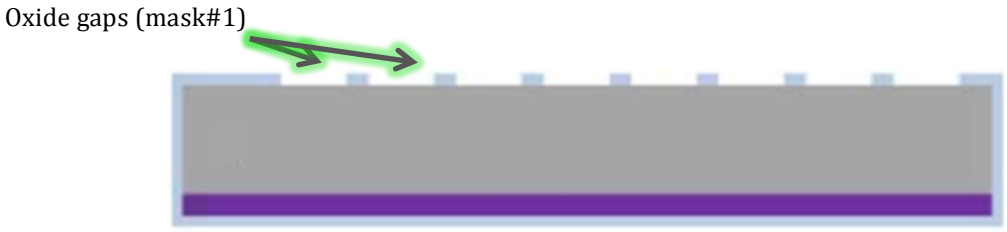

Figure 33 - Wafer after the photolithography of mask#1 [KAI09].

Figure 34 shows the mask used on the process, it may appear that there are two solid squares, but these squares are actually formed of micro-squares between micro-gaps, which will later be exposed to the texturization etch for the creation of the inverted pyramids. It is part of the experiment to only texturize two of the four cells, to study later the texturization effects, so this explains why there are only two squares on the mask.

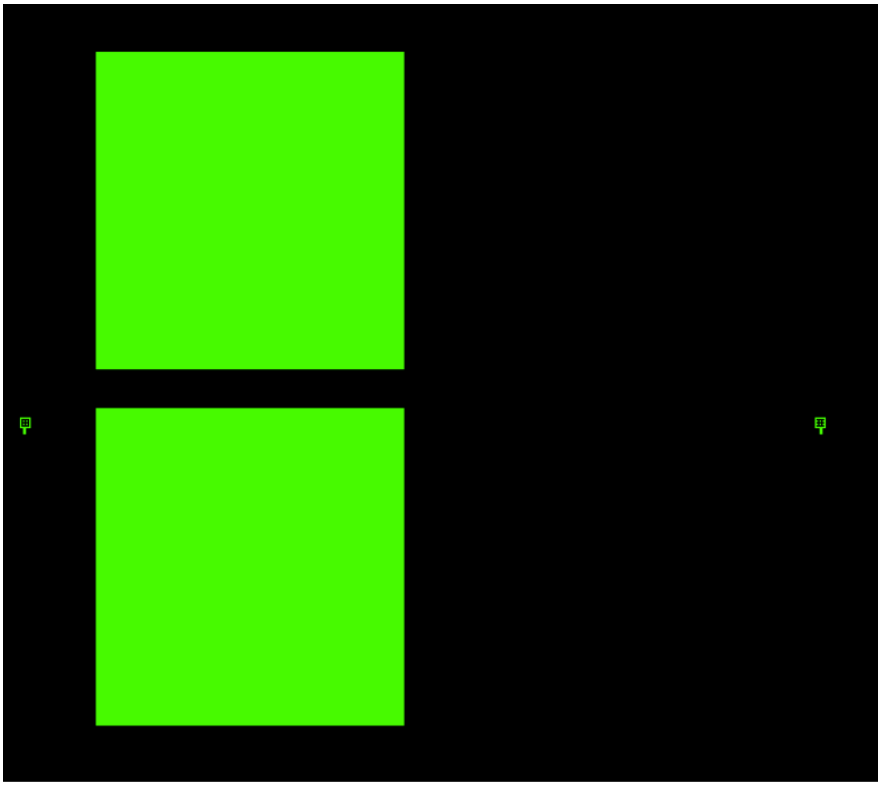

Figure 34 - Photolithography mask#1 [KAI09].

The process started with the deposition of the photoresist (negative), a chemical solution that is resistant to the BOE solution later used to create the inverted pyramids. This photoresist is spared with the assistance of a spin-coater that creates a uniform layer over the wafer's surface. Then, to harden the photoresist, the wafer is soft-baked at a temperature of 115˚C for 60 seconds.

Now, the next step is the exposure of the wafer to the UV light. The exposure takes 4.5 seconds and no alignment is necessary since this is the first mask. The wafer is then submerged on an MF-319 developer solution for one minute. The development step serves to dissolve the exposed photoresist from the surface. As the last part of the photolithography process, the wafer is subjected to the hard-bake, a very important step, which removes any remaining solvents and/or water from the resist. The hard-bake process is very similar to the soft-bake, although, the only difference comes on the time, which, in this case, is 120 seconds at 115˚C.

5.4 Anisotropic Etch & Oxide Etch

The anisotropic etch process is divided in three steps, the first one with the purpose of etching off the SiO_2 from the exposed regions by the photolithography, the second is a cleaning step to remove the remaining photoresist, and the third, to create the inverted pyramids that will help to improve light-trapping and reduce reflectance.

Figure 35 - Wafer after the anisotropic etch [KAI09].

For the first step, the wafer is submerged in a 6:1 BOE solution for 15 minutes to etch off the exposed SiO_2. It is important to remember that the rest of the wafer is still protected by the photoresist that is immune to the effect of the BOE solution. Therefore, the next step cleans off this remaining photoresist with the use of three solvents: *Acetone* to remove the photoresist and *Isopropyl* and *Methanol* to remove the acetone. The wafer is then cleaned with DI (deionized) water and is ready for the texturization.

The third step of the anisotropic etch, the texturization, create inverted pyramids on the exposed regions. For that, the wafer was completely submerged in a TMAH (Tetramethylammonium hydroxide) solution at a temperature of 75˚C for 120 minutes. Finally, the wafer subjected to an oxide etch in 6:1 BOE for 15 minutes to clear off the rest of the SiO_2 layer.

Figure 36 - Wafer after the oxide etch [KAI09].

Before continuing to the next step, a process very similar to the RCA clean descripted in Section 3.2.2.2 is performed to maintain the wafer cleaned of impurities and unwanted solutions. For this process, the wafer is subjected to a bath with the three solutions presented in Table 3.

Table 3 - Cleaning process.

Solution	Composition	Time	Purpose
Piranha Etch	3:1 – 3 HCl to 1 H_2SO_4	10min	Get rid of organic materials
B.O.E.	6:1 – 6 NH_4F to 1 H_2O	10s	Get rid of the native oxide layer in the emitter
-	6:1:1 – 6 H_2O to 1 H_2O_2 to 1 HCl	10min	Get rid of the heavy metal ions

5.5 N+ Front Diffusion & Oxide Etch

The goal of this n^+ diffusion is to create a negative highly doped layer on the topside of the wafer, which will serve to form the emitter on the p-n junction. This process is very similar to the one explained in Section 5.1, but in this case, the source used is phosphorous instead of boron. The wafers were placed onto the quartz boat and loaded into the phosphorous diffusion furnace for 50 minutes at 900˚C. Just like in the boron diffusion, the atoms of phosphorous migrate from the solid sources to the surface of the wafer with the assistance of nitrogen.

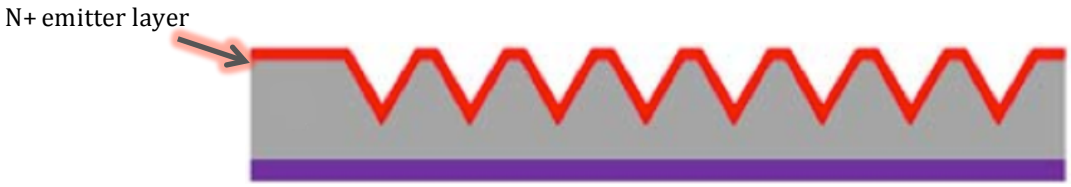

Figure 37 - Wafer after the n^+ diffusion [KAI09].

After the phosphorous diffusion, a layer of phosphocilicate glass was formed over the wafer's surface. This layer needs to be removed, so an oxide etch with 6:1 BOE for 8 minutes is performed to do it. Finally, after the diffusion, the wafer displayed a new value of sheet resistivity, which was measured with the 4-point probe to be 84.16Ω/□ at a current of 6mA. The thermal processing causes the dopants to move further into the substrate, changing the sheet resistivity each time the wafer goes into the furnace.

5.6 Dry Oxidation

This oxidation has the purpose of creating a 0.13µm thick anti-reflective coating over the topside of the solar cells. The ARC serves as a passivation layer and diminishes recombination and reflection. The oxidation is chosen to be dry, because this process ensures a harder and more effective oxide layer. The image below presents an illustration of the solar cell after this stage.

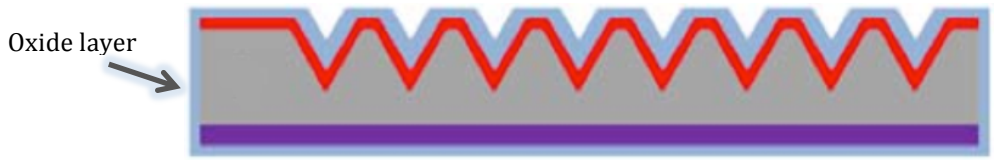

Figure 38 - Wafer after the Dry oxidation [KAI09].

This process is very similar to the wet oxidation, but instead of the oxygen being pumped by a bubbler, it is released directly into the furnace. This process lasted 100 minutes at a furnace temperature of 1000˚C. It is interesting to notice that, after the oxidation, the wafer color became blue and less reflective, while previously it was greyish. The following images present the equipment and the resulted wafer after the dry oxidation.

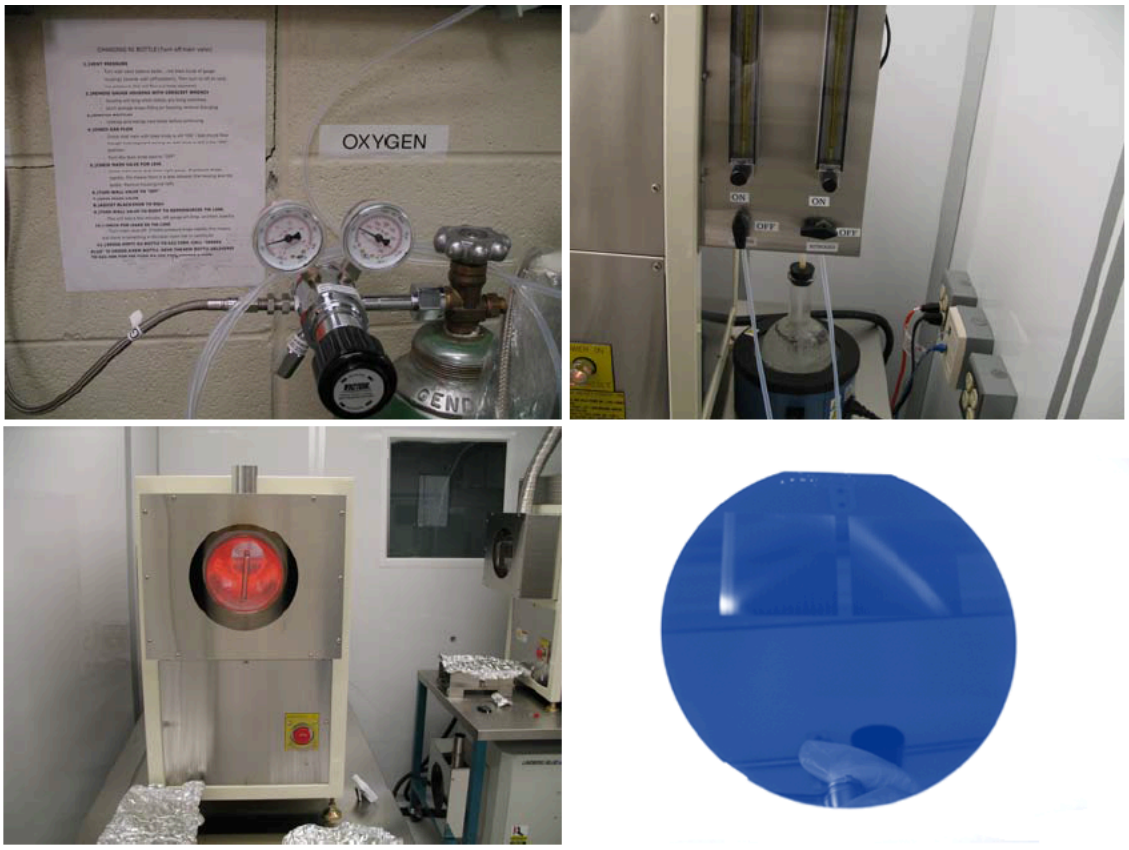

Figure 39 - The oxidation process: oxygen tube, bubbler, furnace and resulted wafer [KAI09].

Since an oxidation was made, the validation of the process is the measurement of the just-created layer. Using the ellipsometer, the oxide layer was measured to be 0.1µm, getting really close to the previewed value.

5.7 Photolithography Masks #2 and #3 & Oxide Etch

The goal of these photolithography steps are to create the pattern for the back and front contacts on the oxide using the masks #2 and #3, respectively. The image below presents an illustration of the wafer after the photolithography processes.

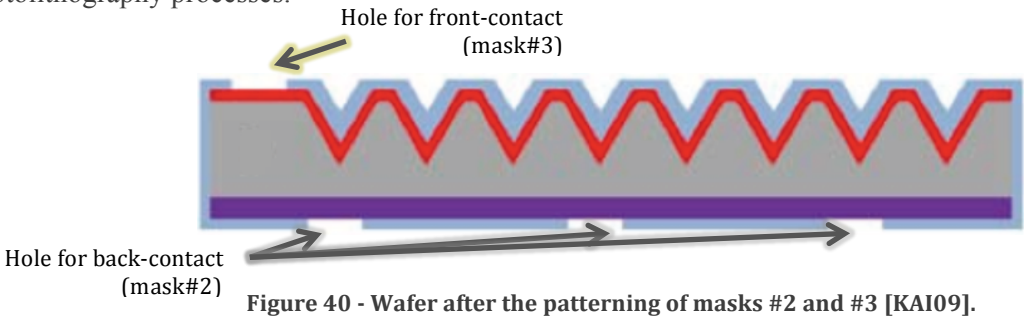

Figure 40 - Wafer after the patterning of masks #2 and #3 [KAI09].

The first mask to be patterned was the mask#2 that had the purpose of patterning the backside gaps on the oxide layer for later depositing the aluminum for the contact creation. This process is the same as the one described in Section 5.3. After the hard-baking step, the same photolithography process was applied to the mask#3, which created gaps to the future front contacts on the oxide layer. It is important to remember that, for mask#3, an alignment step is be added before the exposure.

After performing both photolithography processes, the exposed oxide areas were etched through a 5-minute bath in 6:1 BOE solution to prepare for the creation of the contacts. An image of mask#2 is not available, but Figure 41 presents the mask#3. It is interesting to notice that the mask is divided in two parts, one have solid and visible fingers (top), and the other exposes the whole surface (bottom), removing the ARC layer from those two solar cells as part of the experiment.

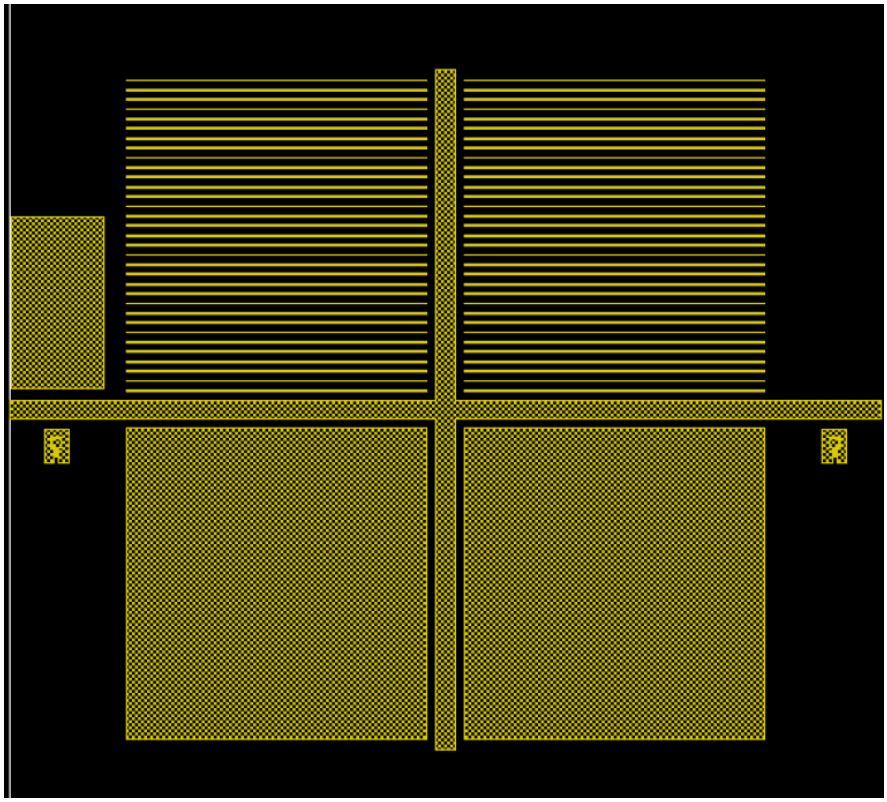

Figure 41 - Photolithography mask#3 [KAI09].

5.8 Aluminum Evaporation (Front)

The main part on the creation of the metal contacts is done by the deposition of the metal over the wafer. In the case of this fabrication process, the deposition method chosen was the aluminum evaporation through the thermal evaportation method.

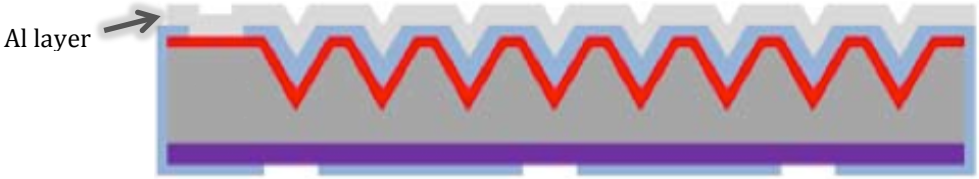

Figure 42 - Wafer after the aluminum evaporation [KAI09].

Before performing the aluminum PVD, a solvent clean just like the one presented in Section 5.4, was performed to clear the wafer from the photoresist and external impurities. Then, as presented in Figure 43, the aluminum filament was placed inside the PVD system being hold by two grips, and the wafer was positioned just above it, with the topside facing the filament. The PVD process occurs by the elevation of the temperature and evaporation of the aluminum filament directly to the wafer. This should provide an Al layer of about 0.6μm thick over the wafer's surface.

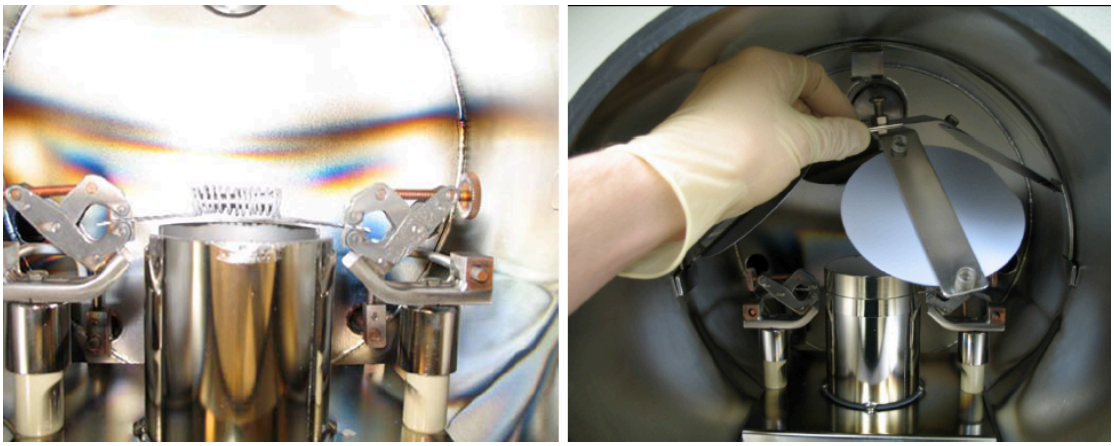

Figure 43 - Aluminum PVD processes preparation [KAI09].

5.9 Photolithography Mask#4 & Aluminum Etch

As the last photolithography step, mask#4 is applied to pattern the front contacts. This process was performed just as the previous ones, which included the photoresist – in this case, positive – application and uniform scattering, the soft-baking for 60s at 115˚C, the alignment, the exposure for 4.5s, the development for 60s and the hard-baking for 120s at 115˚C.

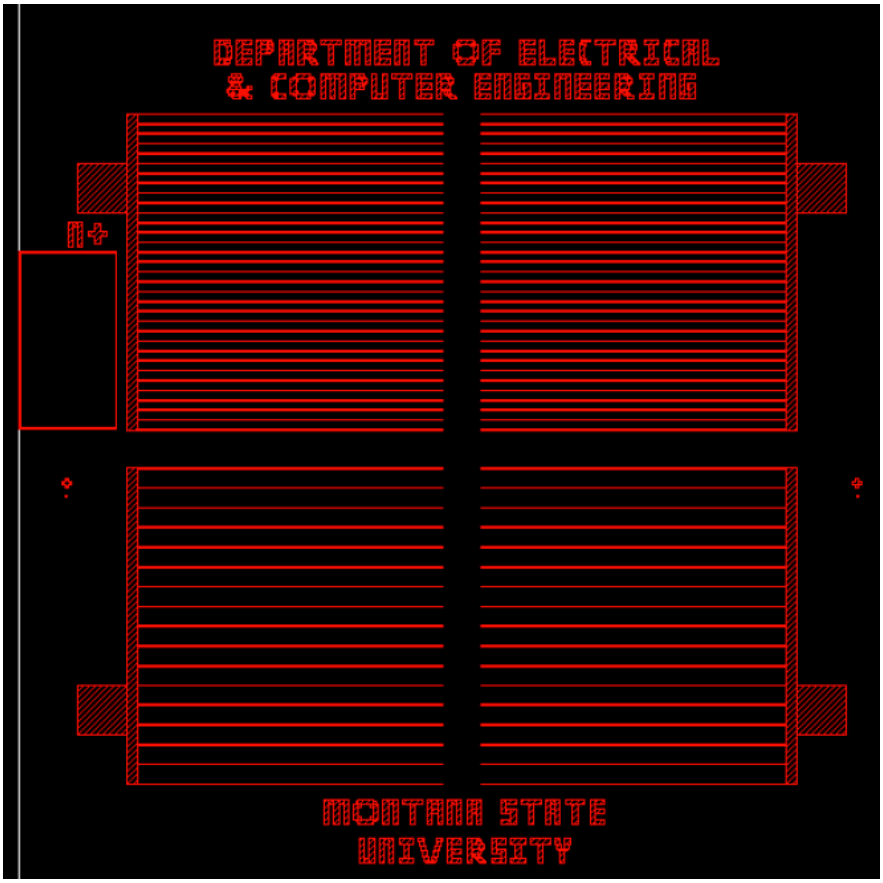

Figure 44 - Photolithography mask#4 [KAI09].

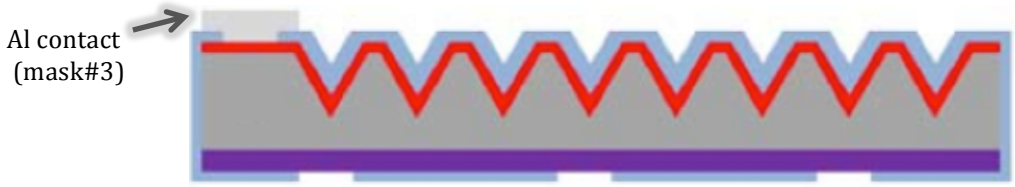

Figure 45 - Wafer after the photolithography of mask#4 and the Al etch [KAI09].

After the lithography process, the Al was etched off with a PAE (Phosphoric Acid Etch) solution that has an etching rate of 0.035µm. Therefore, to remove the entire unwanted Al layer, the etching process was necessary to last about 15 minutes at room temperature. It is interesting to verify that, due to the positive photoresist in this case, the exposed parts were not the ones that were etched off, instead, the exposed aluminum (red parts of the mask#4 - Figure 45) continued on the wafer while the rest was removed.

Later on, the remaining photoresist was removed with a solvent clean process, and the aluminum contacts' thickness were measured with the *profilometer* (Figure 46). This measurement resulted in 0.66µm, thus, remembering that the thickness of the contacts was expected to be 0.6µm, the measured value is very satisfactory.

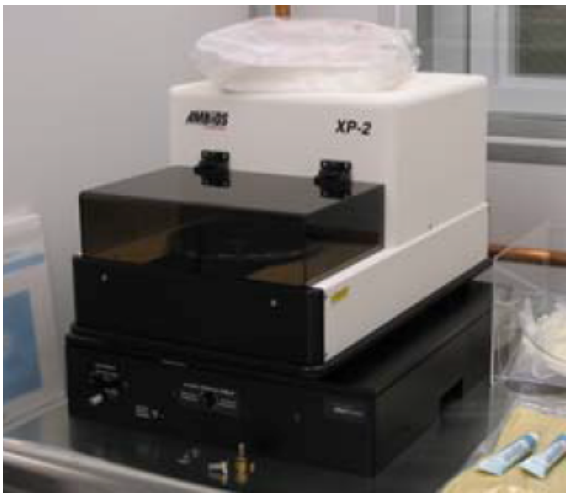

Figure 46 - Profilometer [KAI09].

5.10 Aluminum Evaporation (Back)

The goal of this PVD was to create a thin layer of 0.6µm thick of aluminum on the backside of the wafer. This new layer is the back (positive) contact of the solar cell. The process to create the Al layer is the exact same one as presented in Section 5.8, but in this case, the wafers are positioned with the backside facing the filament.

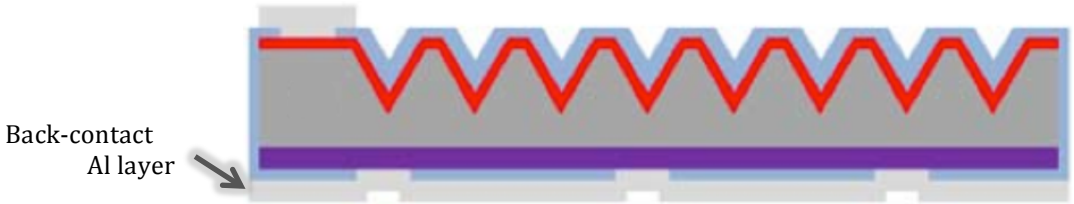

Figure 47 - Wafer after the backside contact creation [KAI09].

5.11 Annealing

At this point, the solar cells fabrication was finished and they are already generating electrical energy through the photovoltaic effect. Although, just after the contacts creation, the aluminum had still a poor connection with the silicon substrate, which led to really low short-circuit currents and open-circuit voltages.

To improve the connection between the contacts and the substrate, an annealing process is applied. This process realizes an inter-diffusion of the aluminum and the silicon through heating the wafer over a hot plate for 60 minutes at a temperature of 400˚C. The image below presents a picture of the fabricated solar cells wafer under annealing.

Figure 48 - Wafer under the annealing step [KAI09].

5.12 Dicing

Dicing is the last step of the fabrication process. It serves to split the four cells off the wafer and enable their use and handling separately. In most cases, this step is performed through laser cutting, but in this situation, it was done by cleaving along the crystal planes with a diamond pencil, and later, roughly crack the wafer on the marks. The red lines highlighted in Figure 49 represent the marks made with the diamond pencil that were later cracked.

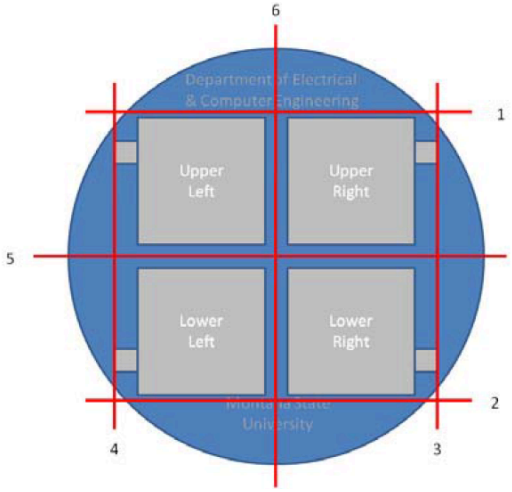

Figure 49 – Red lines represent where was the wafer going to be cracked [KAI09].

5.13 Finished Devices

The fabrication process is now complete and the devices are ready for characterization. The fabricated solar cells are 3.4 x 3.4 cm^2, and none of them have the same design. The table below presents the particular characteristic of each device, pointing the equivalent one in Figure 50. And Figure 51 presents the dimensions of the fingers and bus bars.

Table 4 - Solar cells characteristics.

Device	Wafer Position	Figure	Characteristic
Cell A	Top-Left	(a)	Texturized; have ARC
Cell B	Top-Right	(b)	Not texturized; have ARC
Cell C	Bottom-Left	(c)	Texturized; do not have ARC.
Cell D	Bottom-Right	(d)	Not texturized; do not have ARC

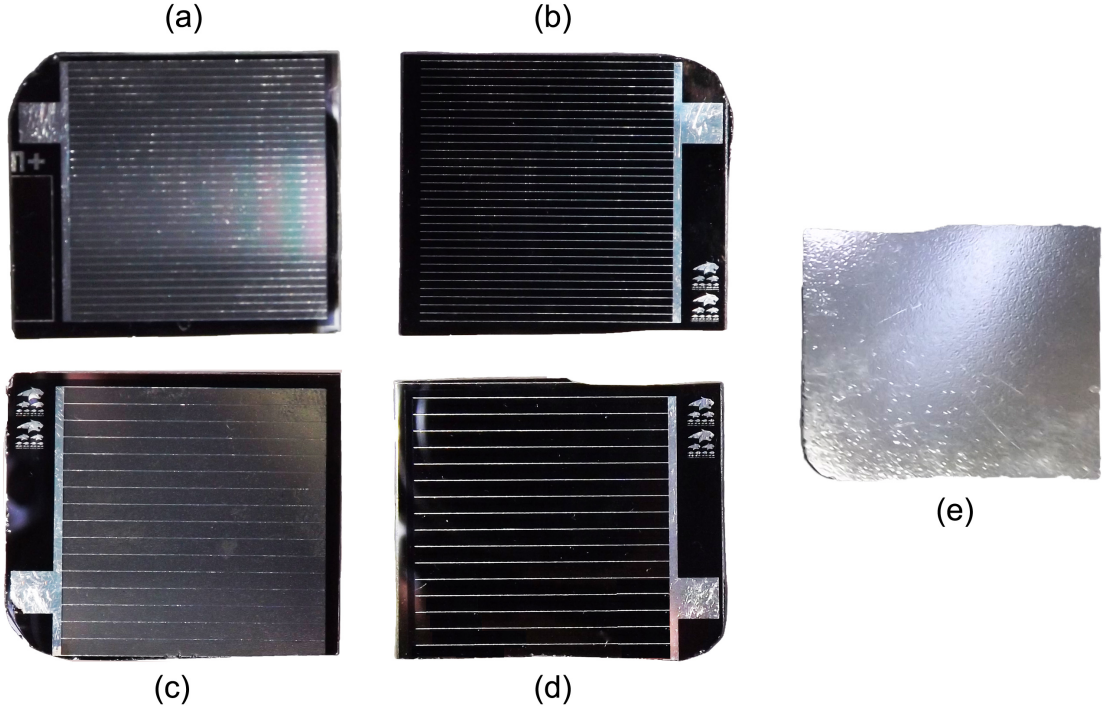

Figure 50 – (a) Cell A; (b) Cell B; (c) Cell C; (d) Cell D; (e) Backside of the cells.

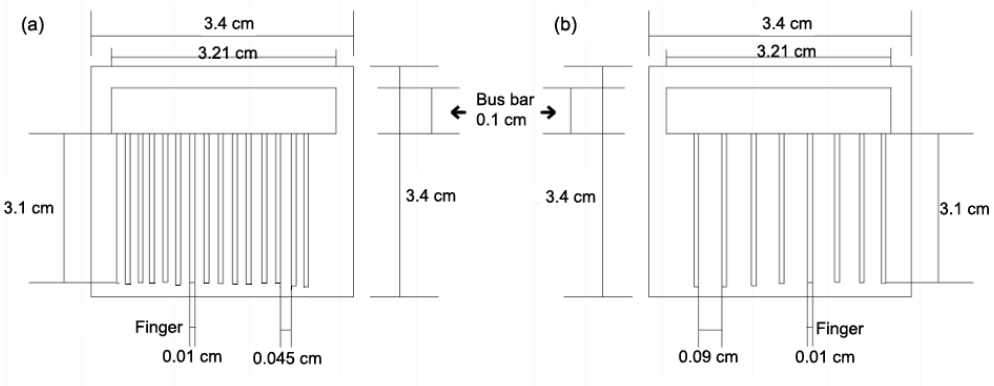

Figure 51 - Contact dimensions of (a) Top cells (A and B) and (b) Bottom cells (D and C).

6 CHARACTERIZATION

This Chapter presents the electrical characterization of the four solar cells fabricated on Chapter 5. These results are then compared to the characterization made to the n^+pp^+ structure in Section 4.2.2.2. And finally, a possible application to the developed solar cells is commented in the last part.

6.1 Characterization

The characterization step described in this section has the purpose of defining the electrical characteristics of each solar cell developed in Chapter 5. This process was done using the *Photo Emission Technology Solar Simulator CT150AAA* located at the NT-Solar in PUC-RS. This equipment measures the most important solar cell's parameters and the I-V curve through the emission of light at certain energy rate.

To perform the characterization process each solar cell was placed, one at a time, in the simulator. The light energy rate defined for the simulation was 1000W/m^2, at a temperature of 25°C and solar cell area of 11.50cm^2. According to the simulations, all the devices work correctly, but their efficiencies were lower than expected. The reasons of this low-performance are explained in the sequel.

The results of the characterization process are shown in Figure 52 and Table 5, which present the I-V curve and the characteristic parameters of each solar cell, respectively.

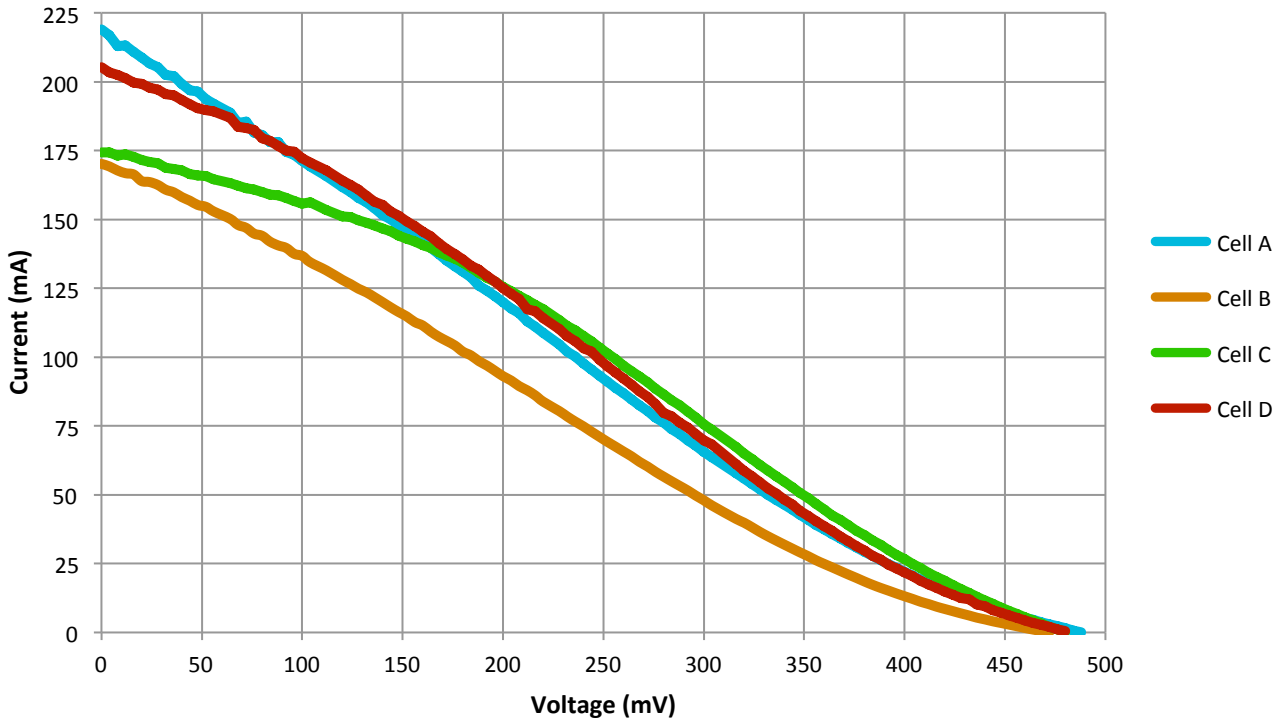

Figure 52 - Solar cells I-V curves.

Table 5 - Solar cells characterization parameters.

	Cell A	Cell B	Cell C	Cell D
V_{OC} (mV)	488.20	472.20	480.70	472.10
I_{SC} (mA)	219.09	170.27	174.96	205.32
V_M (mV)	208.90	202.00	231.30	216.30
I_M (mA)	115.06	92.36	111.88	116.07
M_{PP} (mW)	24.03	18.65	25.88	25.11
FF	0.26	0.23	0.31	0.26
η (%)	1.86	1.45	1.99	1.94
R_S (Ω)	6.00	8.32	4.10	5.1
R_{SH} (Ω)	2.37	1.87	4.78	15.20

The simulation results presented that all solar cells had a similar performance despite their structural differences. *Cell C* stood out over the others with the highest efficiency among them, while *Cell B* presented the worst values in all parameters. This result might not agree with the previous studies, which defined that, theoretically, a solar cell with ARC and texturing should have a better performance than a cell without one or both of them [PVC14]. For example, *Cell A* (have texturization and ARC) might present higher V_{OC} and I_{SC} when compared to *Cell D* (do not have texturization and ARC), but the ratio between its maximum power and its V_{OC}xI_{SC} point is lower, thus, leading to a lower efficiency conversion too.

When analyzing the solar cells fabrication process and comparing to the results, five points come to be relevant to the devices functionality and can explain the reasons for this performance. These are cited and explained as follows.

- *Thick and low-quality wafer substrate* – In most studies of silicon solar cells, the usual wafer thickness ranges between 200µm and 350µm [TOM14][SZL97][MOE12]. In the case of the cells developed in this project, the wafer substrate had a thickness of about 525µm, thus, considered high, especially for a small-area device like the ones presented. Also, the minority carriers' lifetime of the wafer was unknown. Thick substrates, especially, with low minority carriers' lifetime may lead to high bulk recombination rates, which negatively affect the voltage, current and efficiency of the cell [LAW05].
- *Aluminum as a front-contact material* – It is not very common to find aluminum alone as the front-contact material of a solar cell. Normally, these contacts are formed of silver [EBO12]. Despite the fact that it is complicated to solder aluminum for the creation of PV modules, when compared to silver, it presents a conductivity rate almost three times lower [SER98]. Therefore, a device using aluminum as front-contact metal may present losses due to the material's properties.
- *Thin contacts* – When compared to previous studies, the contact thickness used in this project (0.66µm for the front contacts and 0.6µm for the back) is significantly low [AMI94][GRE84]. Thin

contacts lead to increased power losses and high series resistances. Also, studies have shown that, especially on the backside, thick contacts and BSF produce a great increase in V_{OC} [AMI94].

- *Finger spacing* – For such small-area solar cells, having 900µm or 450µm space between fingers is considered excessive. The increased number of 100µm wide fingers and the minimum spacing between them significantly increase the shading losses and the series resistance.
- *Poor contact between the metal contacts and the substrate* – The fabricated solar cells displayed a poor contact between the metal and the substrate. This fact directly influences to the increase of recombination near the metals and parasitic resistances. The ideal procedure to avoid this problem would be to strongly dope the contact regions in the substrate.

After this previous analysis on the fabrication procedures versus the results of the solar cells, it is possible to conclude that the main reason to the limited performance of the devices are the high recombination rate and the parasitic resistances (especially the series resistance), both caused mainly due to the faulty structure of the contacts. Returning to Table 5, it is possible to notice that *Cell C*, the most efficient one, has the lowest value of series resistance and the second highest value of shunt resistance when compared to the others. Also, *Cell D* presents the second best relation of parasitic resistances, leading it to the second highest efficiency among them.

6.2 Comparison

To situate the performance of the devices fabricated in this project with industrial solar cells, this section presents a comparison of the highest efficiency device developed (*Cell C*) with the highest efficiency n^+pp^+ cell fabricated at PUC-RS and mentioned in Section 4.2.2.2. This solar cell was chosen, especially, because it's structure is very similar to the one presented in Chapter 5. Figure 53 presents the comparison graph between the two solar cells, and Table 6 compares both structures characteristics.

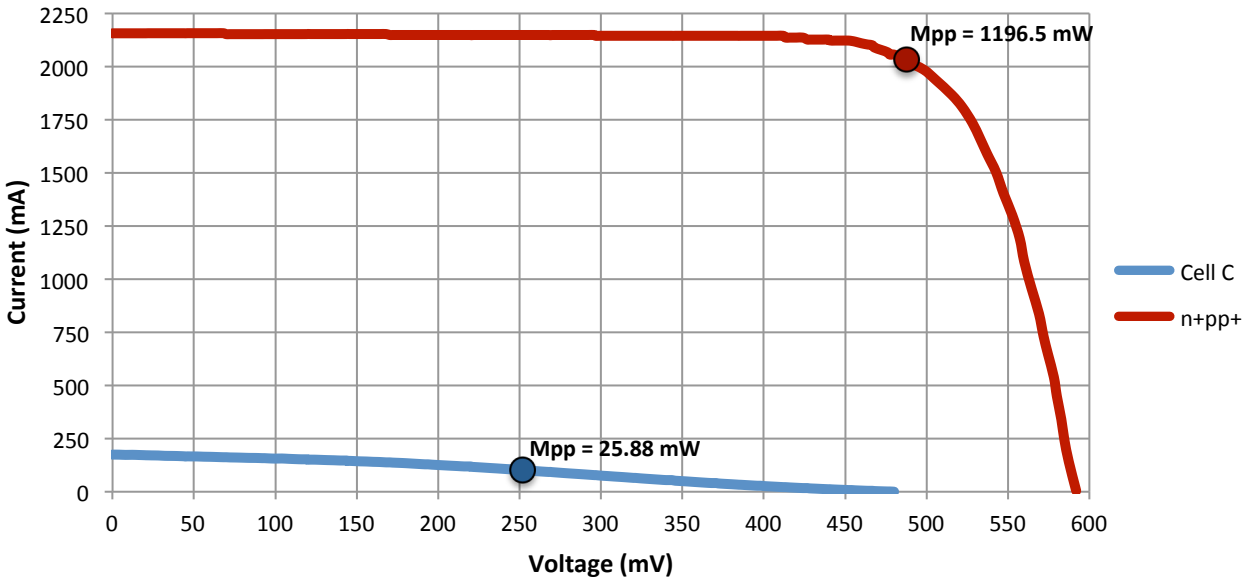

Figure 53 - Solar cell comparison.

Table 6 - Comparison of the Cell C and the n^+pp^+ cell structures (information on the n^+pp^+ cell taken from [MOE12]).

	Cell C	n^+pp^+	Notes
Substrate	525µm thick cz-Si	300µm thick cz-Si	Thicker substrates with low minority carriers' lifetime can increase bulk recombination [LAW05].
Junction	Phosphorous diffusion	Phosphorous diffusion	The p-n junction process used was the same.
ARC	SiO_2	TiO_2	TiO_2 presents a lower reflection rate than SiO_2, thus, generating a more effective ARC [RIC03].
BSF	Boron diffusion	Aluminum diffusion	-
Front Contacts	Al 100µm wide and 0.5µm thick	Ag 100µm wide and 18µm thick	Ag has a better conductivity rate than Al and is easier to be soldered [SER98]. Also, thicker contacts diminish series resistances and reduce power losses.
Back Contacts	Al	Al/Ag	Ag has a better conductivity rate than Al and is easier to be soldered [SER98]. In the n^+pp^+, Al is still used to reduce costs.
Other layers	SiO_2 layer between the BSF and back contacts	SiO_2 layer between the ARC and emitter	For both cells this serves as a passivation layer.

Verifying the previous analysis, it is notable the expressive advantage of the n^+pp^+ cell over the solar cells fabricated in this project. The device presented by Moehlecke *et al* displayed an efficiency of 16.1% [MOE12] against only 1.99% of the *Cell C*, and a much higher V_{OC} and I_{SC}. Also, this device exhibited a much better substrate thickness, anti-reflective coating material and front and rear contacts.

It is important to highlight that the device developed at the NT-Solar was fabricated in a pilot scale, with well-trained personnel aiming a desirable efficiency rate. Meanwhile, the devices presented in this project were fabricated during an academic course, which had the main purpose of only introducing the fabrication processes and technology to the students.

6.3 Application

Due to the limited performance of the developed solar cells, especially in comparison to actual cells industrially produced, it was not possible to find any application. An output power of 25.88mW (*Cell C*) is too low to be applied in any electrical scenario. Also, some experiences were made by trying to use the devices in series mode, but no success was achieved, the output power stilled too low, especially because the solar cells have a fair efficiency discrepancy between each other, making the series setup not very effective.

7 Conclusion and Future Work

This project presented a compilation of the most important topics on the solar cell technology, along with the analysis and evaluation of the performance of four solar cells fabricated by the author through a laboratory process sequence during an exchange university program in the United States. This compilation goes from basic concepts to fabrication methods and high efficiency structures, including the detailed process sequence used on the four solar cells fabrication, their characterization, industrial device comparison and possible application.

On the fabrication of the four solar cells, the author used a sequence of laboratory processes composed of successive photolithography sessions and chemical etches with the purpose of applying four masks: the first for the creation of squares for texturization, the second and third for the back- and front-contact holes, respectively, and the fourth, for the patterning of front-contacts metal. These devices were all created in one single wafer and later diced into 3.4 x 3.4 cm^2 solar cells for their separate testing.

The characterization of these devices revealed a poor performance with low open-circuit voltages, short-circuit currents and efficiencies ranging from 1.86% to 1.99%. This behavior was caused especially due to the faulty contact structure of the cells, which had very thin contacts, leading to increased series resistance and low shunt resistance.

Nevertheless, it was made a comparison with the n^+pp^+ solar cell, a device developed by *Moehlecke et al* through an industrial process in the NT-Solar. The results proved that this solar cell performance is extremely superior to the devices fabricated by the author, showing efficiencies around eight times higher. Also, some experiences were made, including setting the devices in series mode, to find a possible application to the fabricated solar cells, but, due to their poor performance, it was not possible to create any application scenario.

Finally, it is important to highlight that the purpose of this work was not only to evaluate the performances of the fabricated solar cells, but also to learn deeply the photovoltaic technology and its state of the art, which is not taught in the computer engineering course in PUC-RS. Also, the solar cells fabricated and presented in this project were developed during an undergraduate course and did not have the purpose of achieving high efficiencies or surpassing any other existing electrical energy generating device. The main goal of the fabrication of these cells was acquiring the experience on the development processes of the technology.

7.1 Future Work

The solar cell technology is in constant growth and has been receiving increased attention in Brazil, especially due to the great amount of solar irradiance this country receives. An interesting future work to this project would be to introduce the principles of this technology to the computer engineering undergraduate curriculum in PUC-RS. Another important approach to the introduction of the subject to the students and faculty would be the development of a project between the school of engineering (FENG) or the school of informatics (FACIN) in partnership to the NT-Solar, enabling undergraduate students with interests in the subject to participate.

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