SoC-WiMed: Wireless SoC for Medical Monitoring of Vital Signs with a Focus on Security and Low Power Consumption

Porto Alegre, Brazil
May 29, 2025

Goal of the SoC-WiMed Project

- Develop a SoC for vital signs monitoring with **3 subsystems**:
  - biomedical signal acquisition
  - digital signal processing, including AI-based processing and encryption
  - data transmission using Bluetooth Low Energy (BLE)

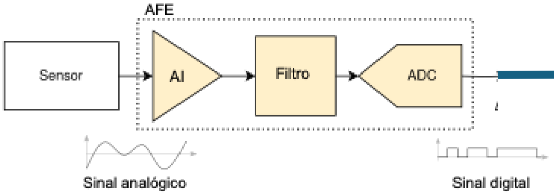
- Balance between performance, security, and power consumption

- **EnSilica** proposed the SoC-WiMed project and has an interest in the technology transfer of the solutions developed within the project

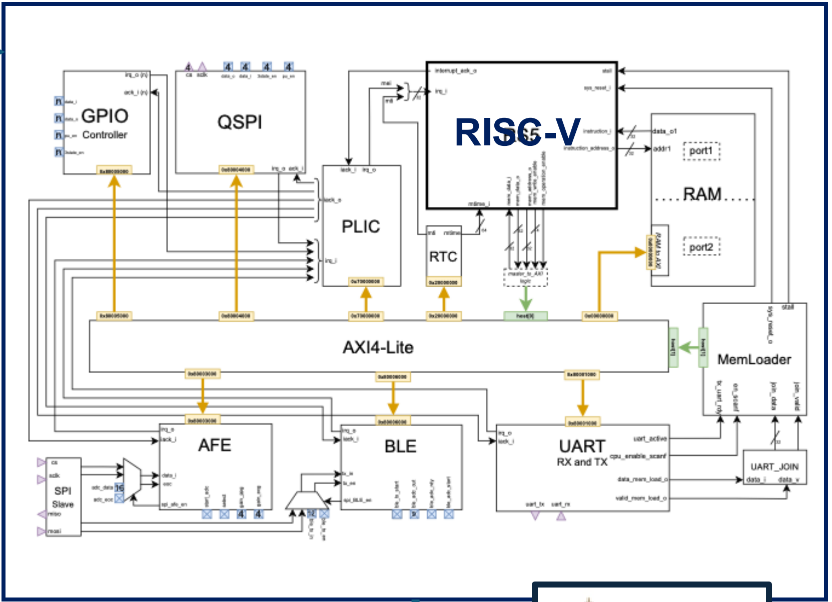
smart watch

smart ring

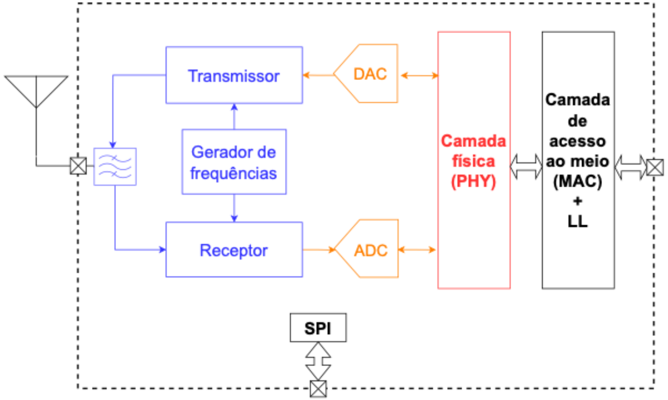
Overview of the SoC-WiMed



unipampa

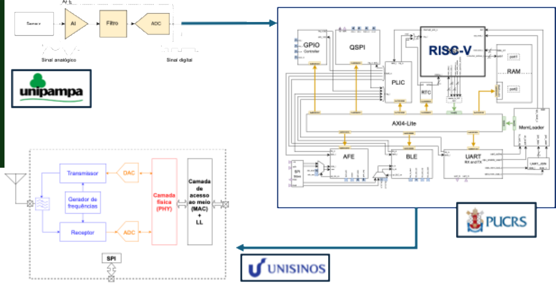


PUCRS



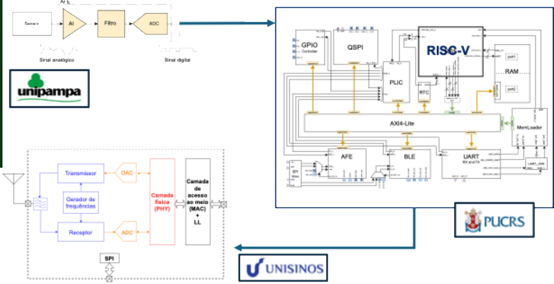
UNISINOS

SoC-Wimed



- integration of different technologies – analog, digital, and RF
- Hardware fully developed within universities, with **no use of third-party IPs**
- Training of **human resources** in microelectronics
- Innovative solution featuring **low power** consumption and enhanced **security** for IoT
- Potential for technology transfer to the industry

SoC-Wimed



- Project team, including students and faculty: ≈ 30 people involved
- NDA signed with TSMC – 28nm technology
- PDK configured and synchronized across the three institutions
- Defined acquired signals: PPG (photoplethysmography) and ECG (electrocardiogram)
- First tapeout planned for August 2025

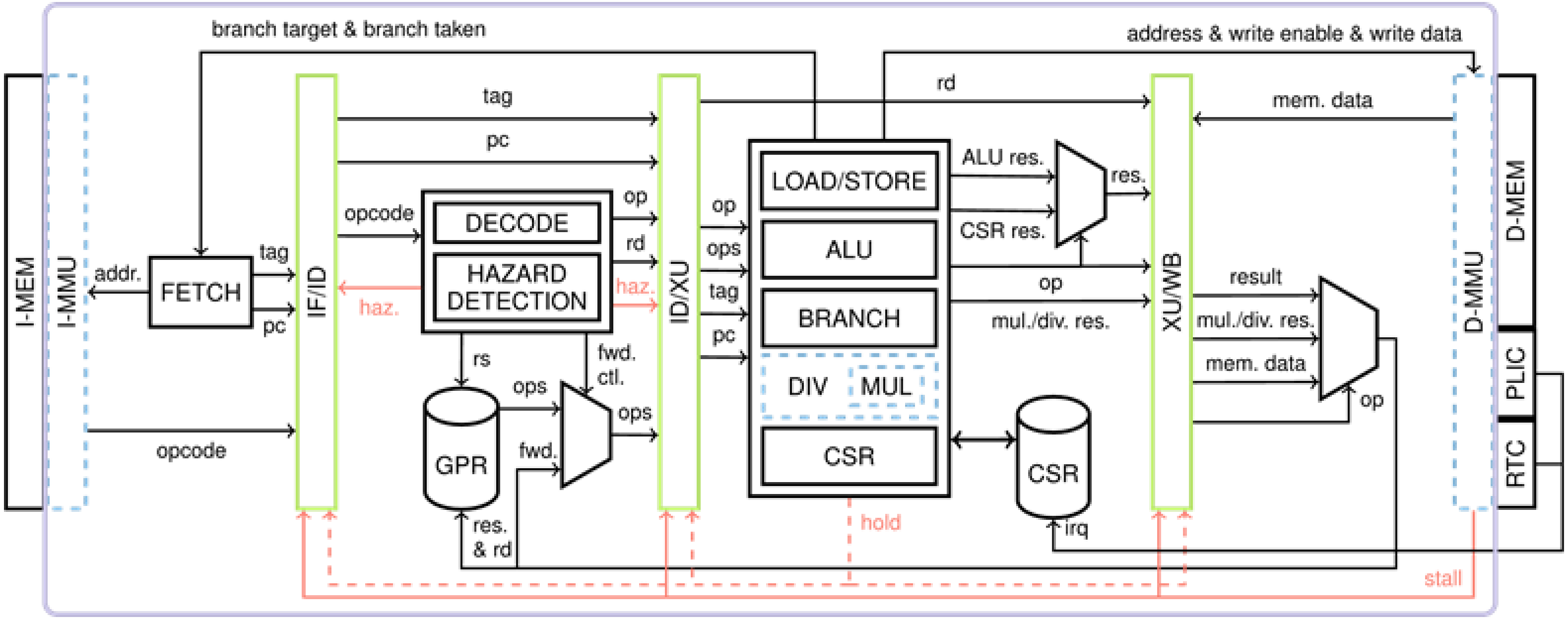
36-month project
2-3 *planned tapeouts*

Bloco Digital (PUCRS)

PUCRS

RISC-V processor – **RS5** – RV32IMAC + Zkne + Zicsr + U/M Modes

https://github.com/gaph-pucrs/RS5



W. A. Nunes, A. E. Dal Zotto, C. da Silva Borges and F. G. Moraes,

RS5: An Integrated Hardware and Software Ecosystem for RISC- V Embedded Systems, In: LASCAS, 2024

Hardware:

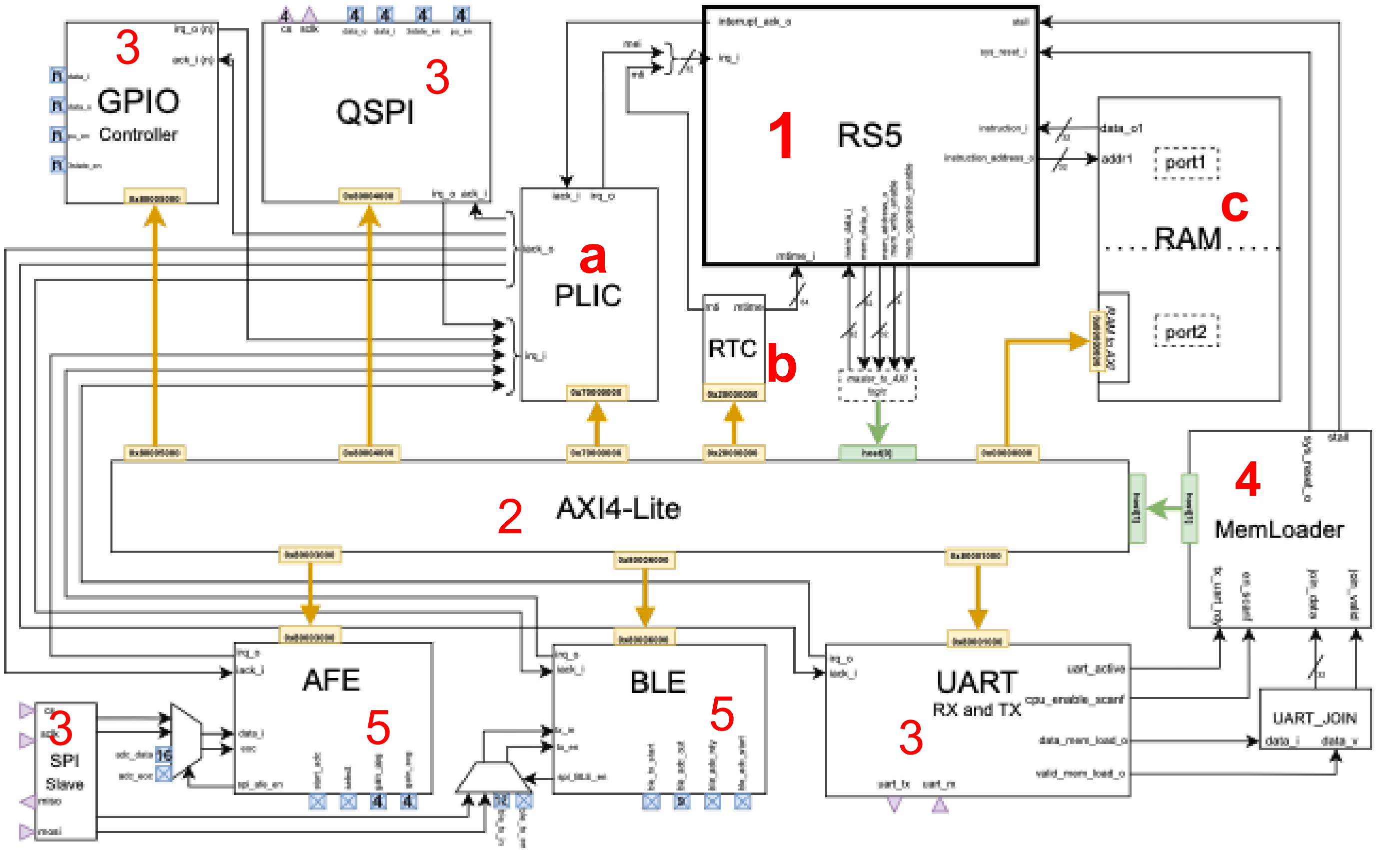
1. **RS5 - RV32IMAC**
   a. PLIC
   b. RTC
   c. Memory

2. **AXI-Lite bus**

3. **UART /SPI / GPIO / QSPI**

4. **MemLoader**

5. **Interface with other subsystems – AFE and BLE**



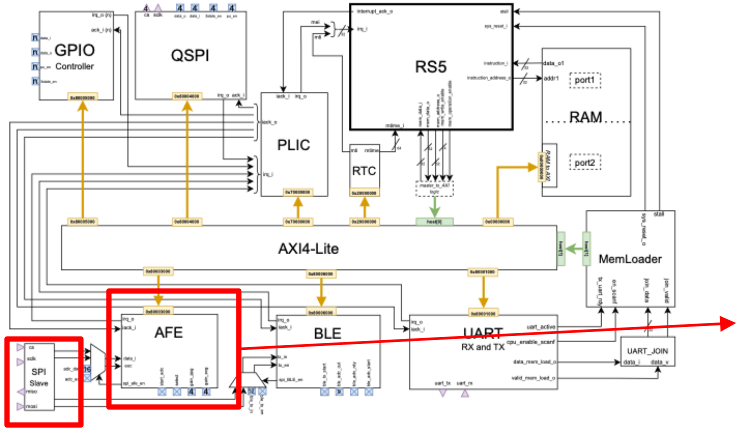
Software - Zephyr RTOS

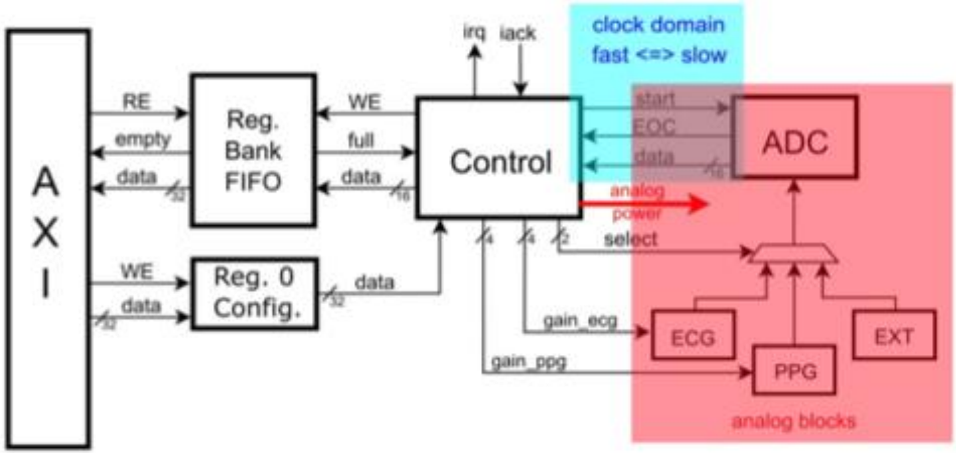
- Deployment of the open-source Zephyr OS
- Low memory requirements (< 20 KB)
- Configuration and development of drivers
- Bluetooth support
- Multitasking capability

Zephyr®

Integration with the analog system

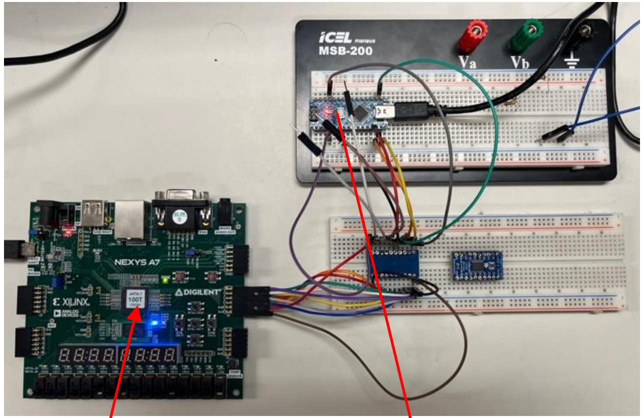
- Peripheral specification defined
- Hardware and software implemented
- Testing through **emulation** of data transmitted via SPI

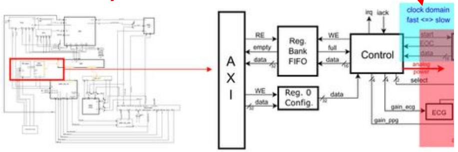


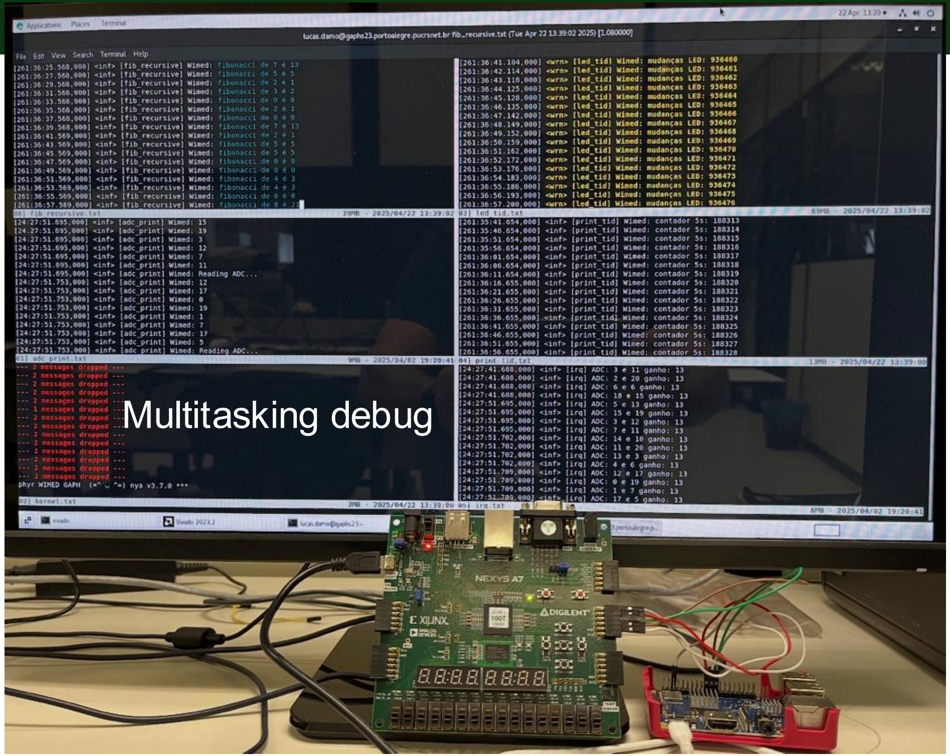


FPGA Prototyping

- FPGA Artix7 (@100MHz)
- Arduino – simulates low-frequency ADC data





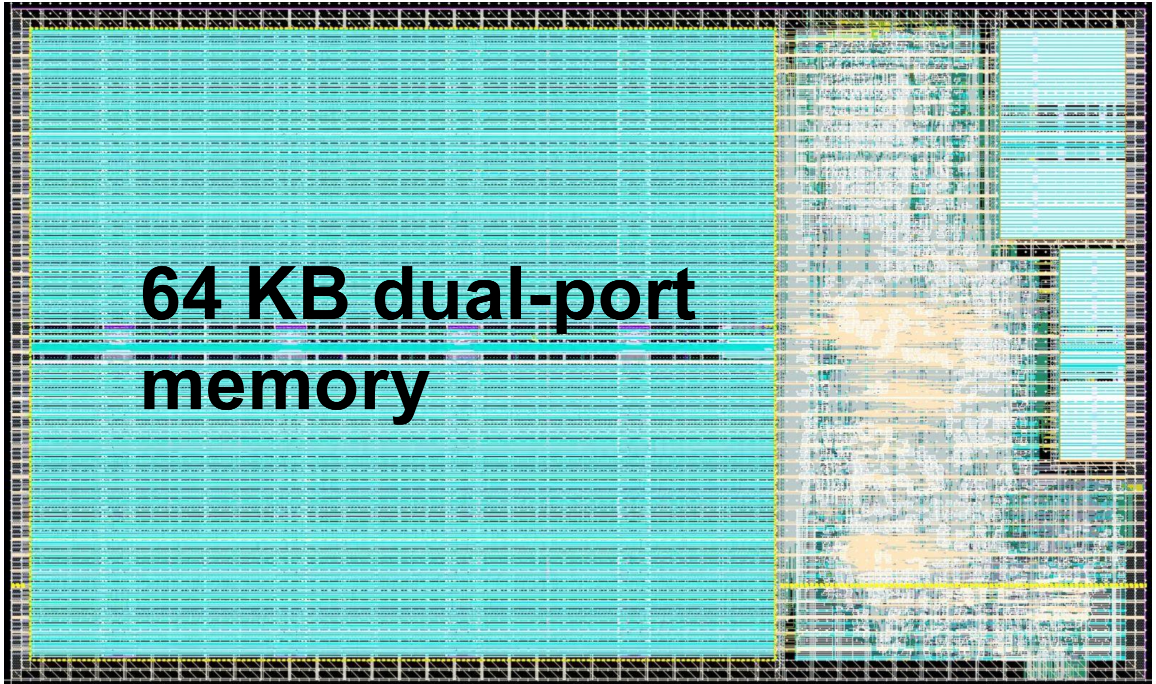


Arduino

USB-Serial connection
AES 128-bit encryption (Zkne)

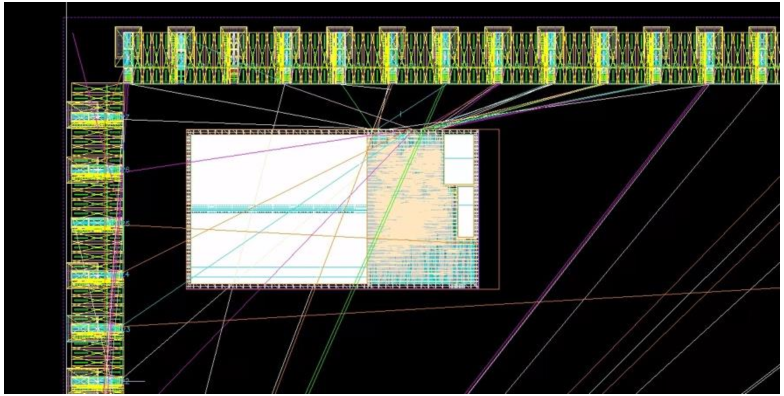
ASIC Implementation

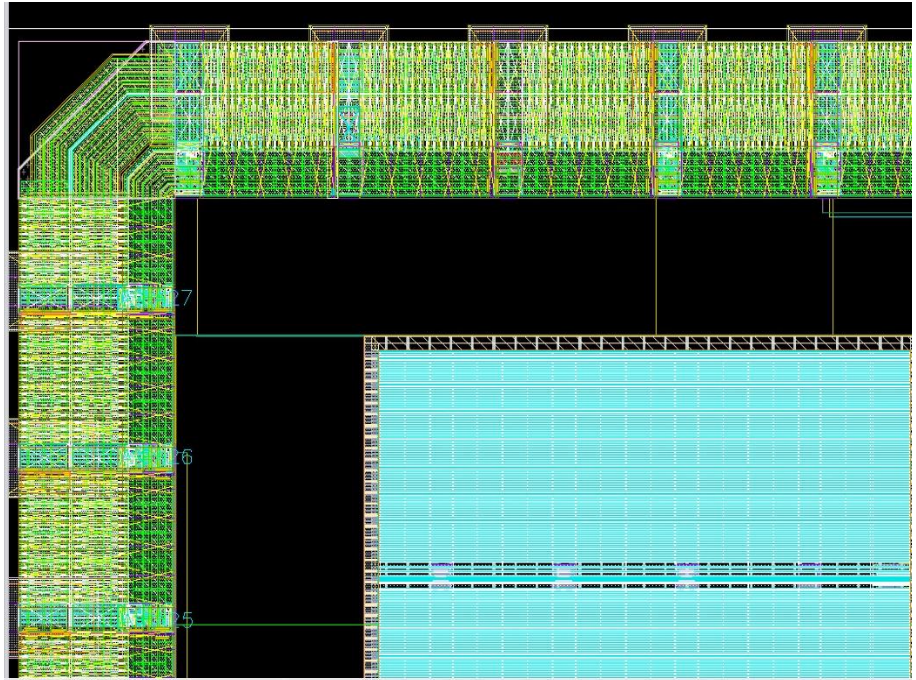
- Post-synthesis simulation with physical memories @256MHz in the 3 corners - signoff ok (setup/hold)
- GDS: 620 µm x 380 µm



ASIC Implementation

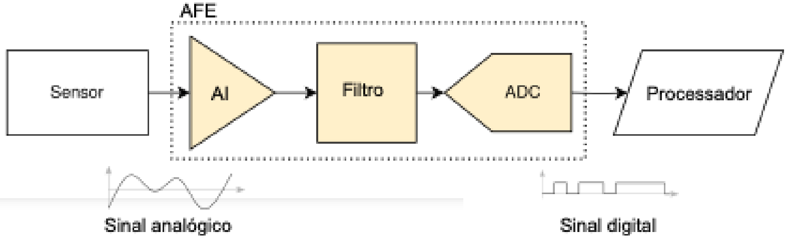
- Analog on top – integration with the pad ring

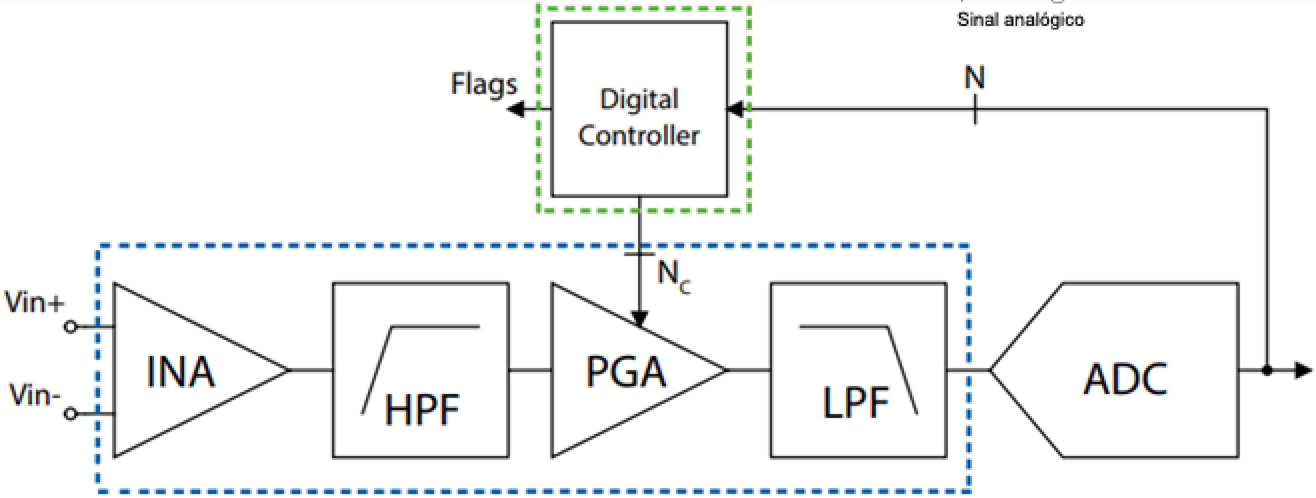




Analog Front-End

Electrocardiogram (ECG)



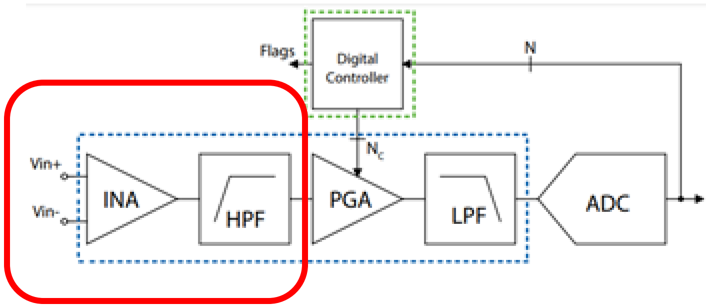


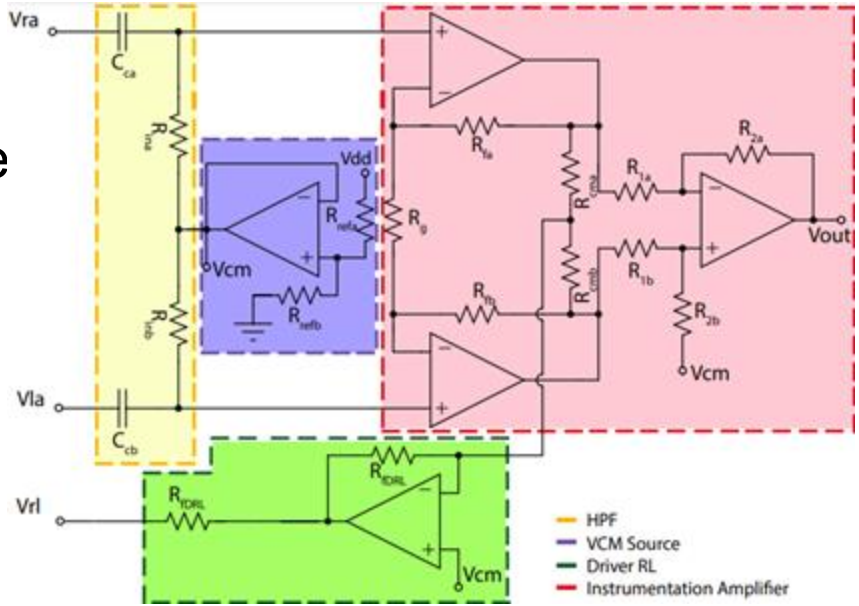
instrumentation amplifier

programmable gain amplifier

Instrumentation amplifier

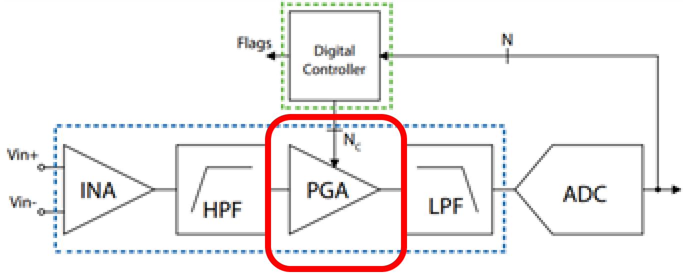
- 3 electrodes (2 inputs and 1 output)
- Requires high common-mode rejection ratio
- Integrated high-pass filter to eliminate body potential
- Requires the design of 5 operational amplifiers





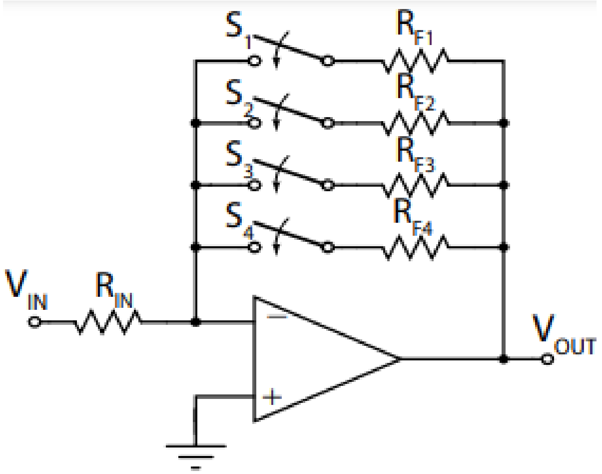
→ current status: layout verification

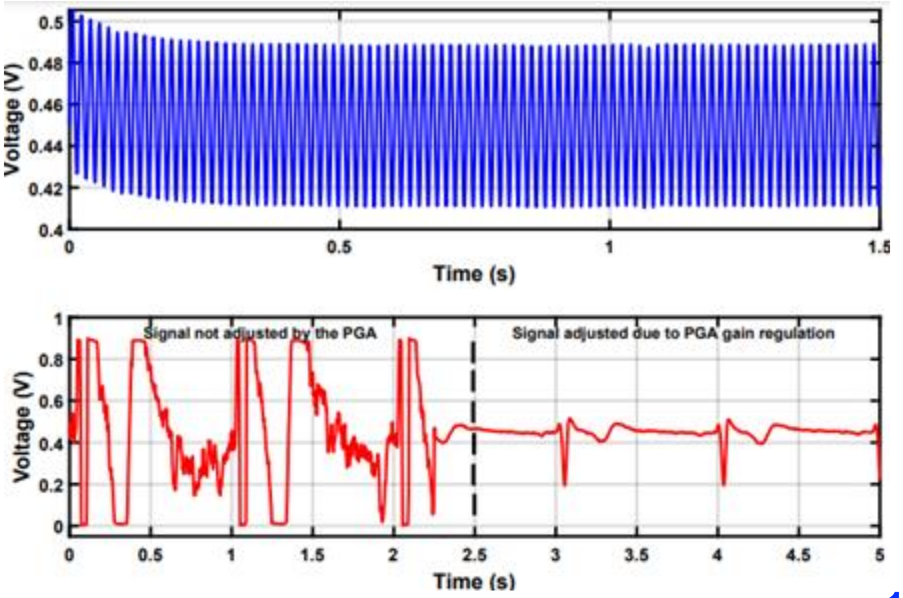
PGA - programmable gain amplifier



- Amplify the signal acquired by the INA.
- The PGA is controlled by the processor that adjusts the gain of the inverting amplifier upon detecting saturation in the ADC output signal
- The gain adjustment is performed by a circuit that modifies the state of switches, allowing the amplifier gain to be changed.

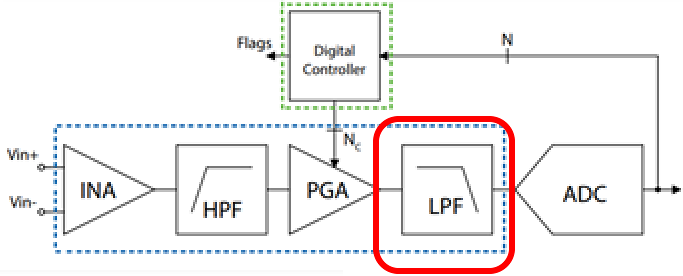
→ processor controls this module

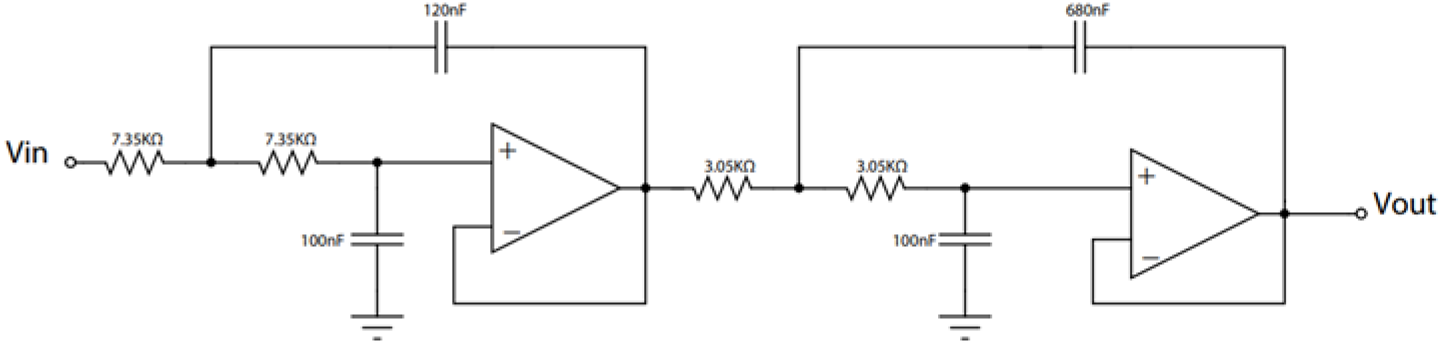




→ current status: layout verification

Low-pass filter





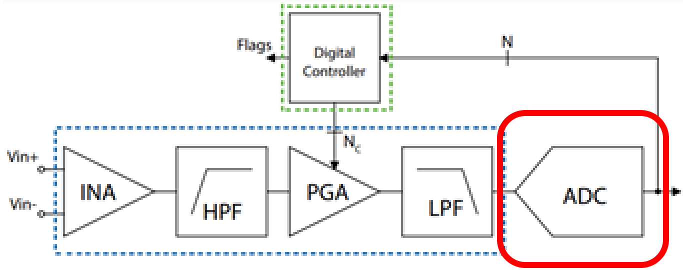
- Fourth-order biquadratic Butterworth low-pass filter (250 Hz)
- Sallen-Key low-pass topology

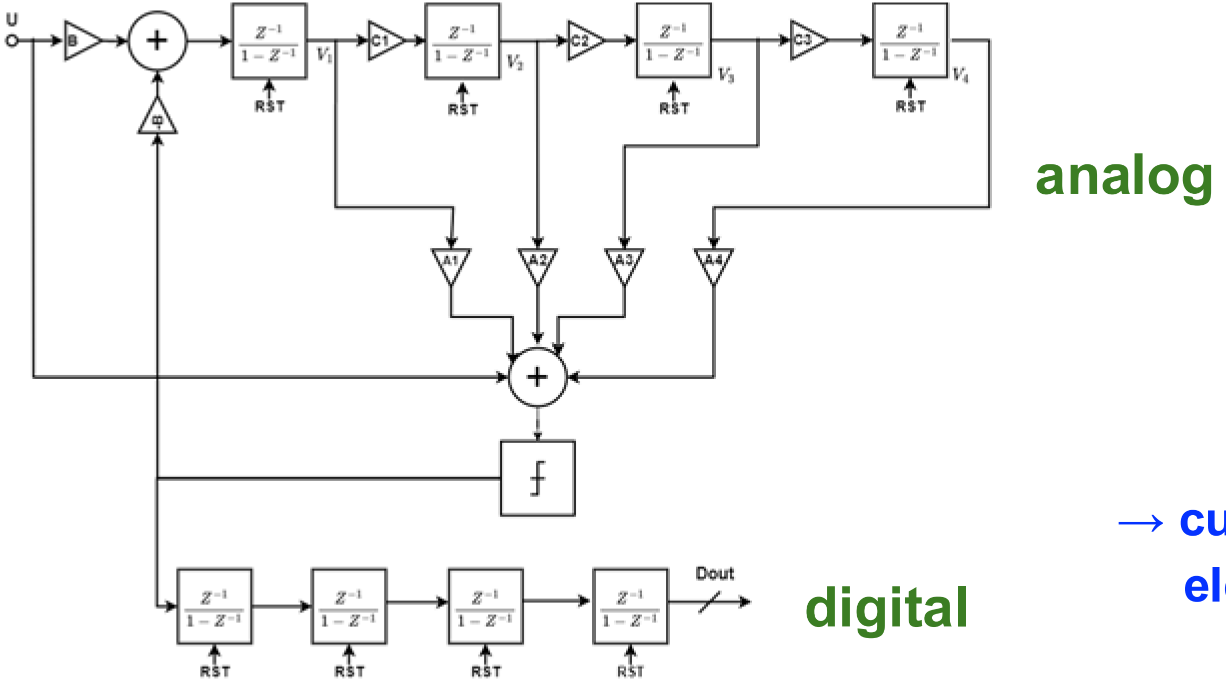
Objective: minimize aliasing effects and ensure proper ADC operation by filtering out all unwanted frequencies from the analog signal before sampling

→ current status: layout verification

ADC – Incremental Sigma-Delta

- Design and simulation validated in **Matlab**
- Fourth-order modulator with >22 bits of ENOB
- Target: 16-bit ENOB and 500 samples per second (sps)



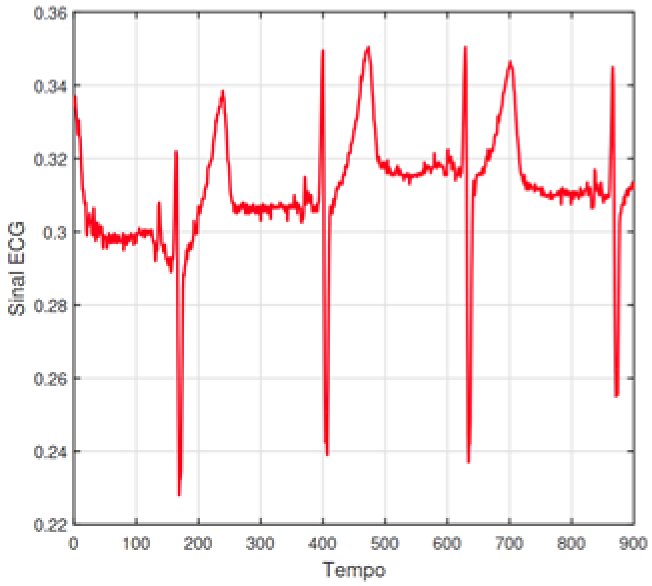


→ **current status: electrical simulation**

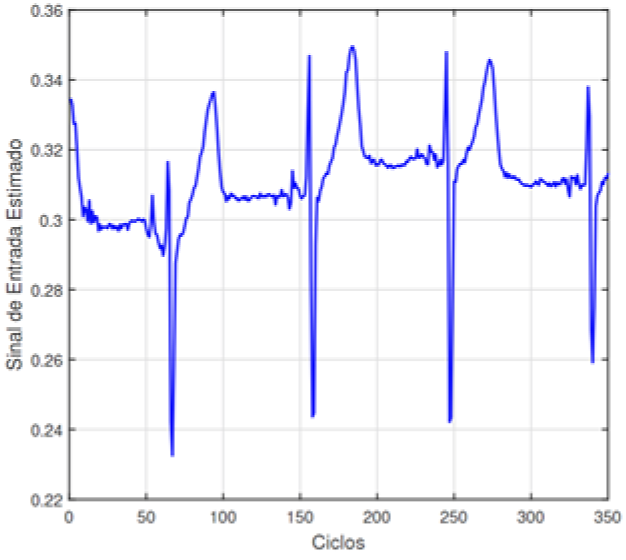
ADC – Incremental Sigma-Delta

- Design and simulation validated in **Matlab**
- Fourth-order modulator with >22 bits of ENOB
- Target: 16-bit ENOB and 500 samples per second (sps)

Input ECG signal



Digitized ECG signal converted to analog



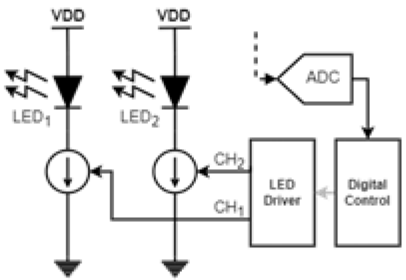
Photoplethysmography (PPG)

Sensor used to detect changes in blood volume through optical signals

Composed of three parts:

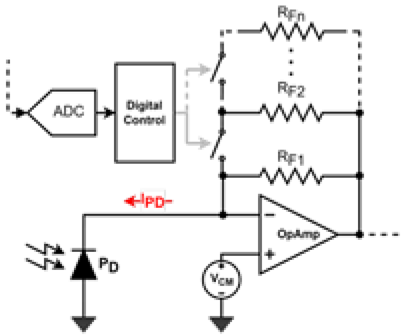
LED Driver

- Controls the current through the LEDs
- Adjusts the minimum saturation level of the ADC



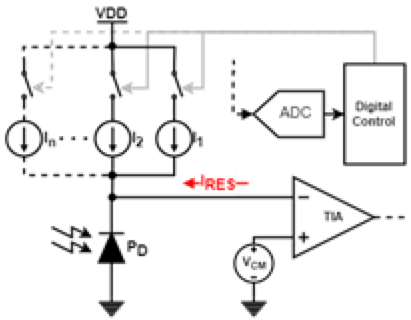
Feedback Resistance

- Adjusts ADC saturation by selecting the feedback resistance.



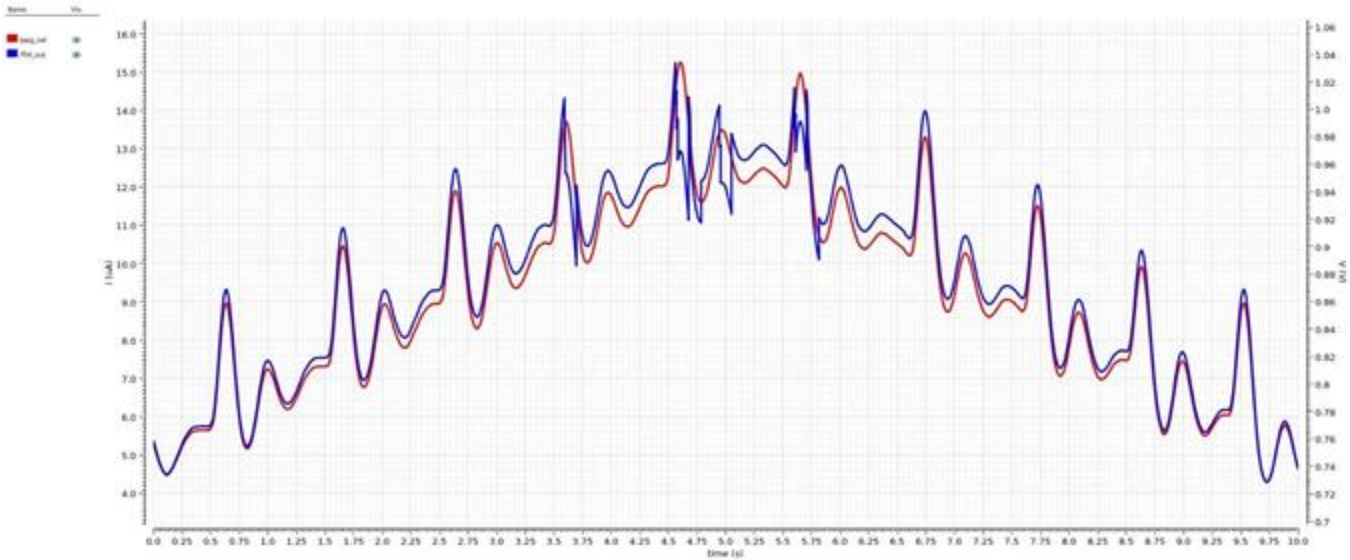
Current Compensation

- Controls the current injected into the transimpedance amplifier.
- Adjusts the maximum saturation level in the ADC



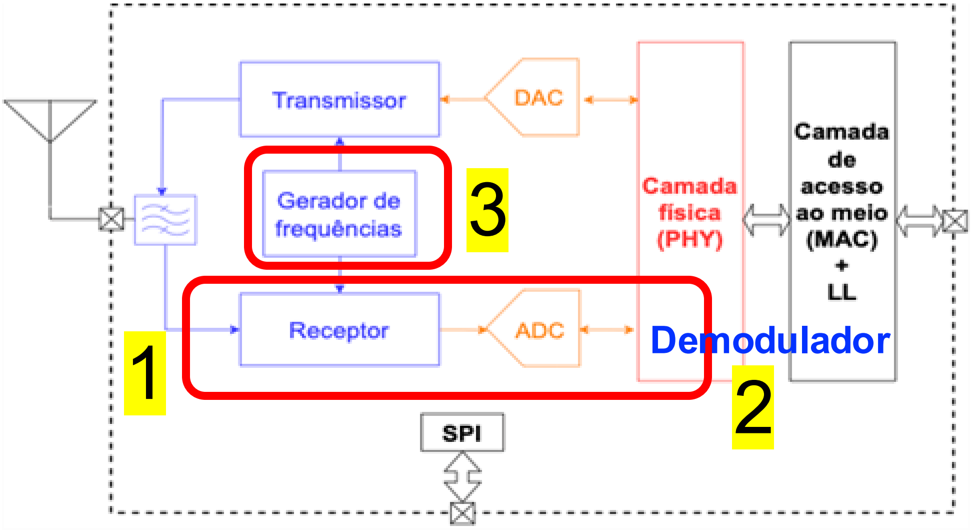
Photoplethysmography (PPG)

- Simulation of the acquired optical signal
  - Red: ideal signal
  - Blue: signal acquired with saturation compensation

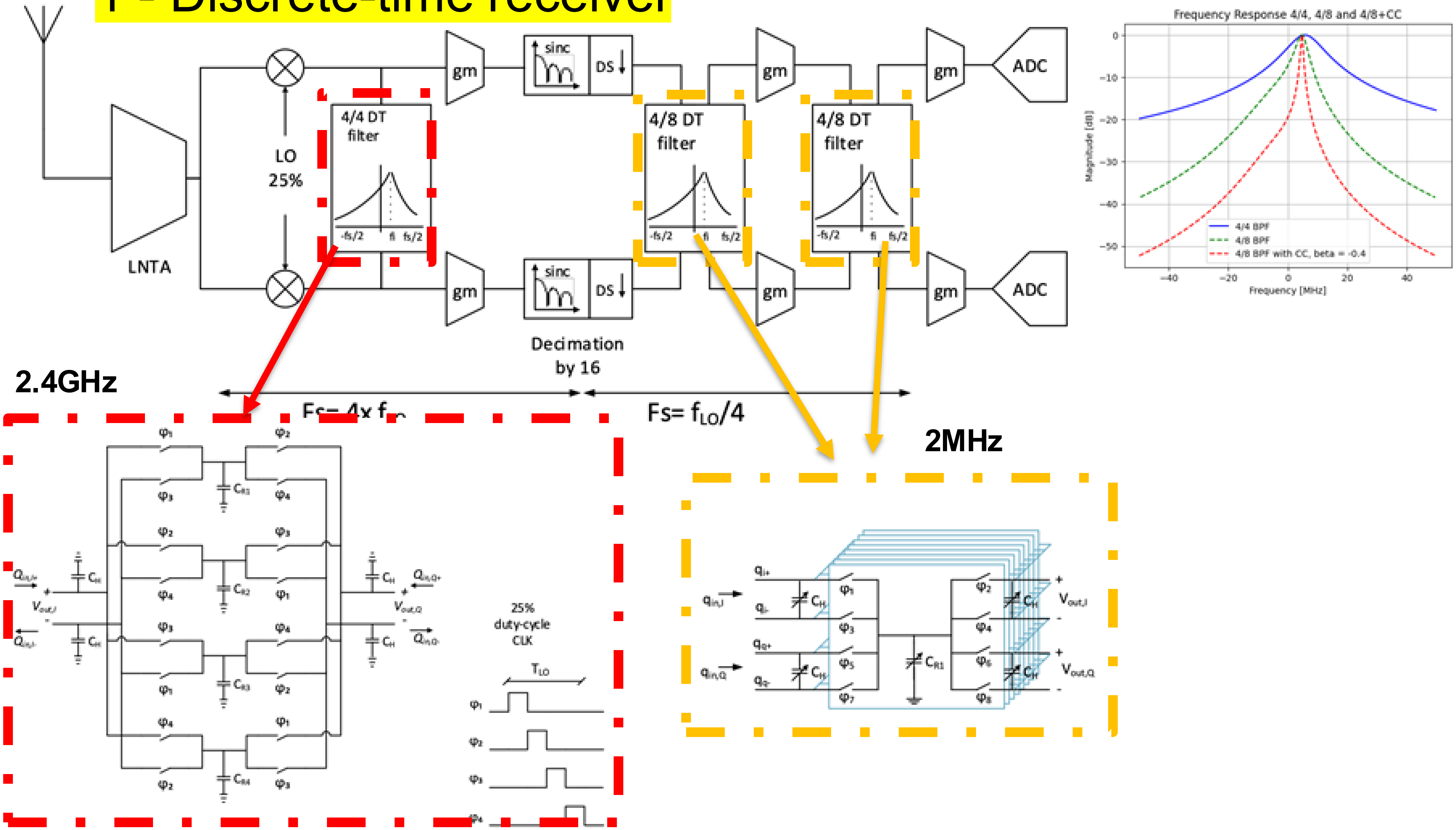


→ status : MATLAB simulation

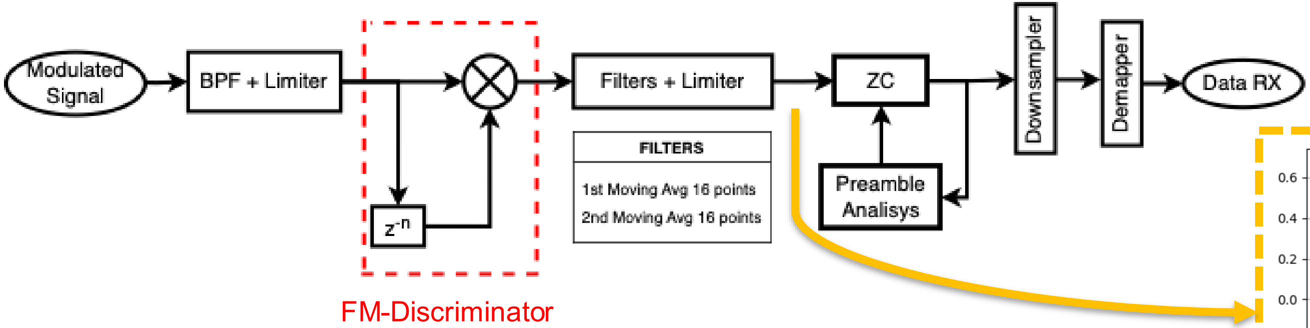
RF Receptor

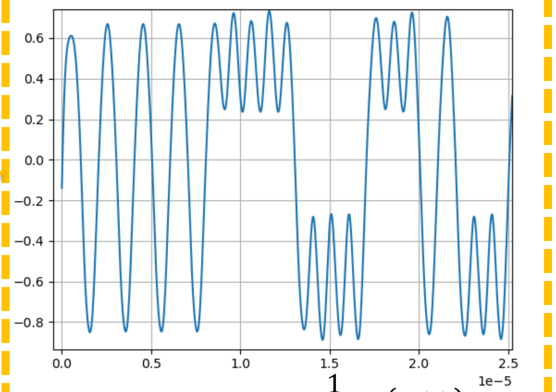

Transmissor
DAC
Gerador de frequências
3
Camada física (PHY)
Camada de acesso ao meio (MAC) + LL
Receptor
ADC
1
Demodulador
2
SPI

1 - Discrete-time receiver

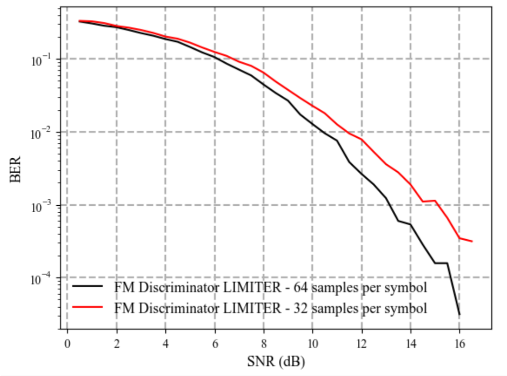


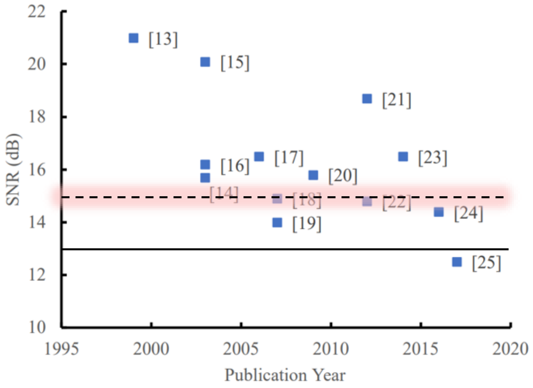
2 - Digital Demodulator





$$LPF\{V_{disc_{out}}(t)\} = \frac{1}{2}\cos(\phi(\tau))$$

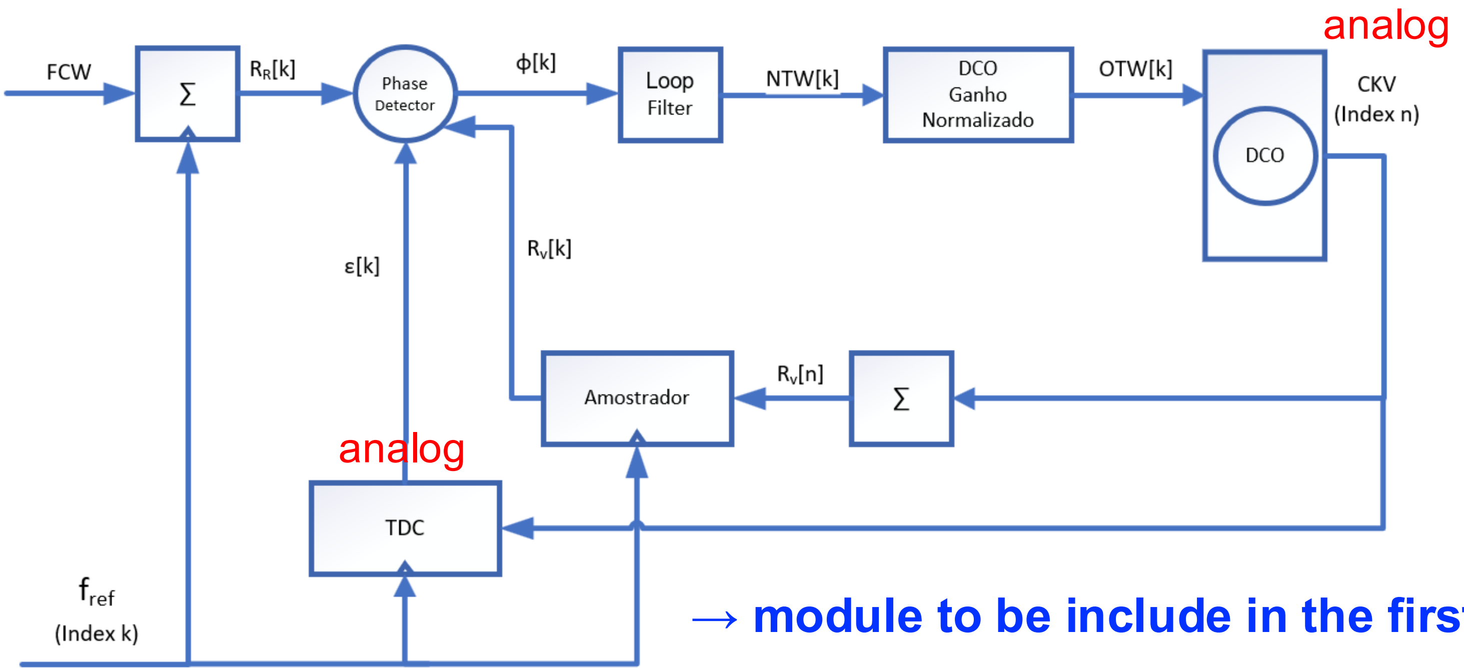




3 Frequency Generator

→ ADPLL - All Digital Phase-Locked Loop

- Operating frequency range: 4.3 to 5.2 GHz
- In-band phase noise: < -91 dBc



→ module to be include in the first tapeout